HIGH POWER NANOSECOND PULSE GENERATOR

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Circuit Description

Presented circuit generates pulses of widths <= 3ns and amplitudes <= 2kV under 50Ω load impedance. The circuit takes advantage of a Drift Step Recovery Diode (DSR) and a saturable core transformer.

Fig.1 illustrates the prototype of this circuit during its measurements and Fig.2 depicts its schematic diagram.

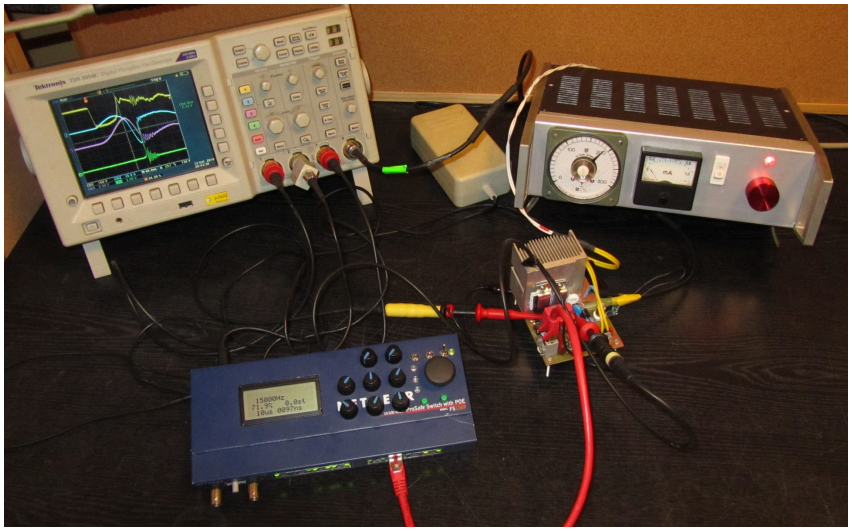


Fig.1: The prototype during measurements.

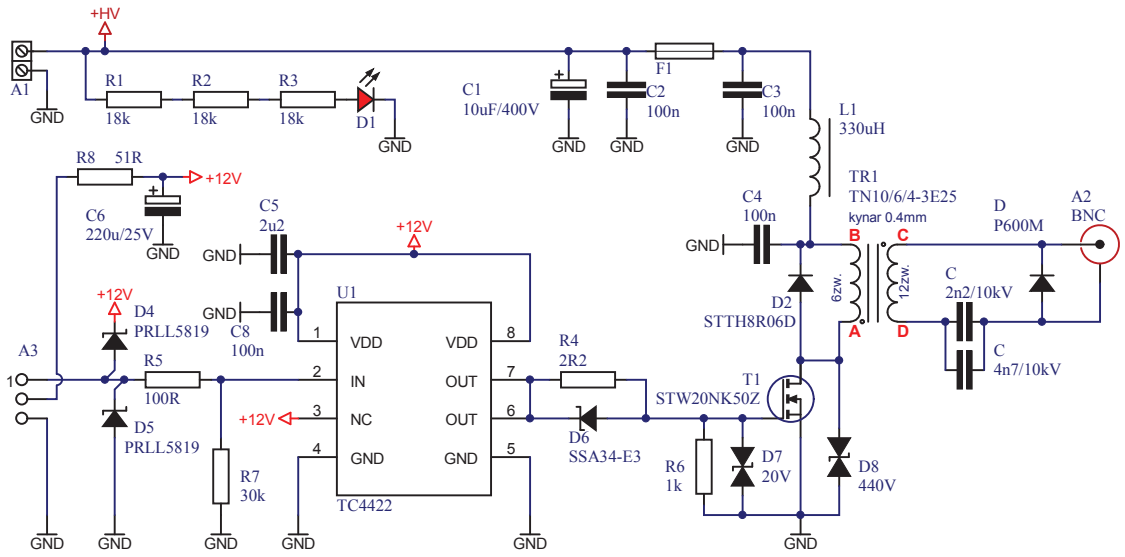


Fig.2: *Schematic diagram.*

Fig. 3 depicts waveforms occurring during pulse generation. The yellow waveform represents the voltage on the drain of T1, the blue waveform represents the current of the DSR diode D,
The violet waveform represents the voltage across the series capacitor C and the green waveform represents the generated pulse measured by a fast high-voltage probe 1:250 (that scope input is not additionally attenuated).

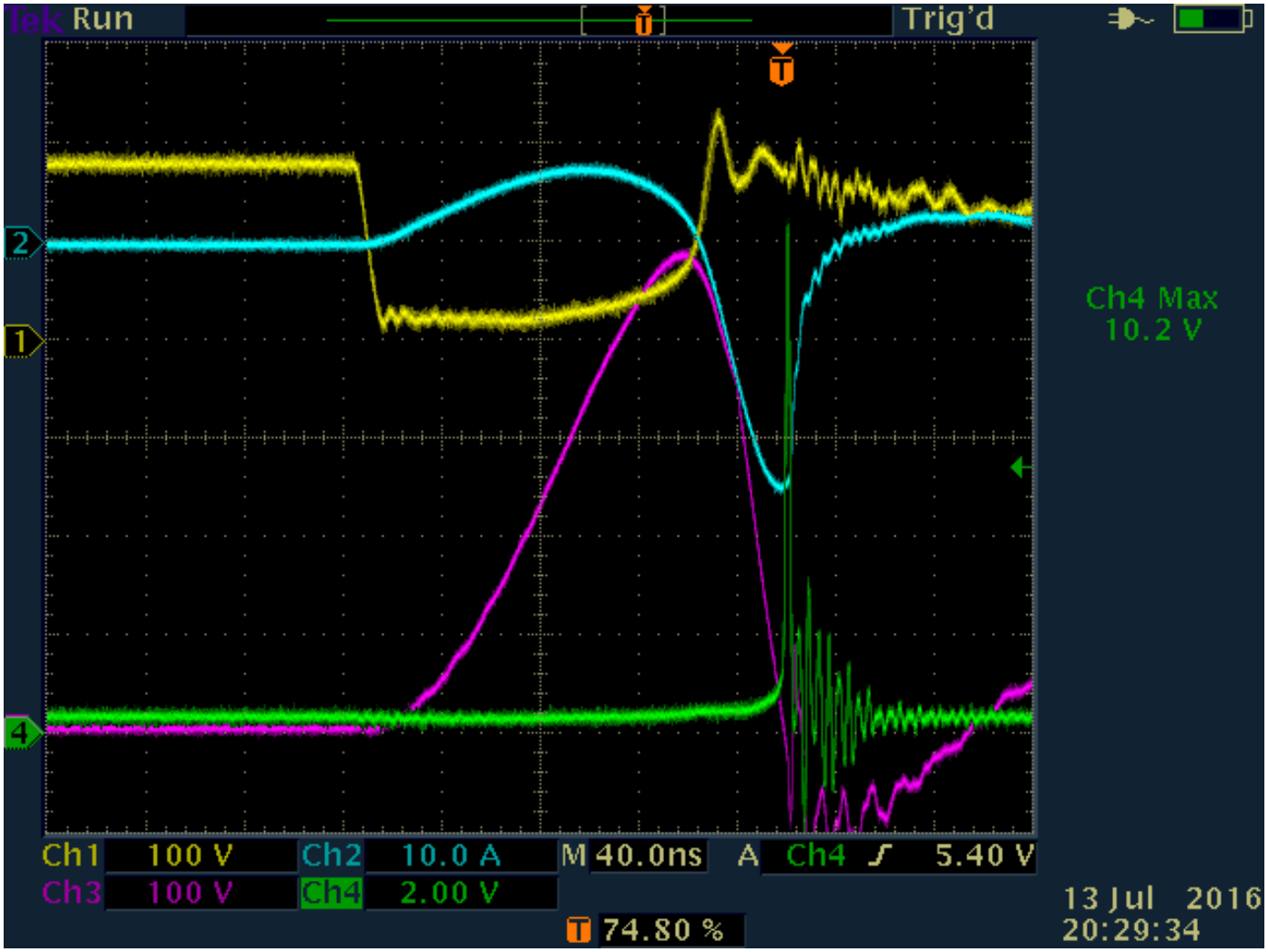
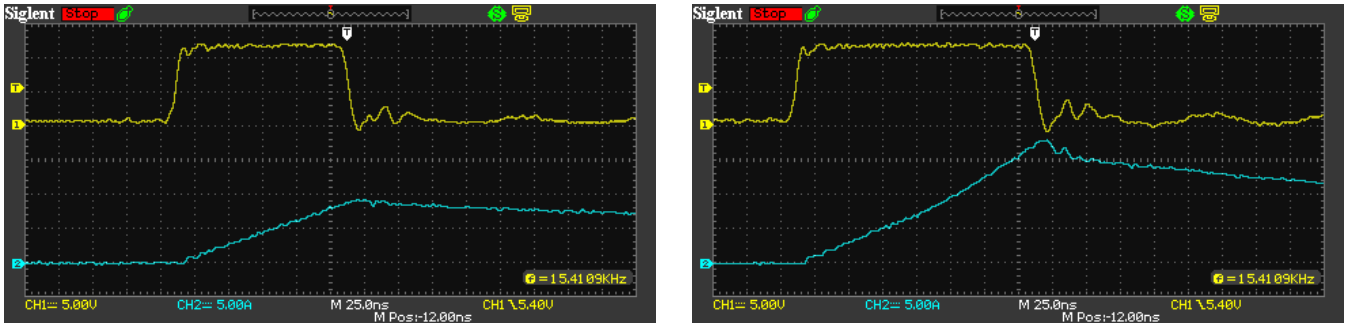


Fig.3: Circuit's waveforms.

This circuit's theory of operation was described in the Russian publication by Belkin and Szulzenko [1] and it served as a basis for construction of the generator descrebed herein.

The input of this circuit expects a short pulse that turns on the transistor T1. In response to this, a current starts to flow in the secondary circuit of TR1, C and D while the diode is forward biased. This current is sinusoidal (the blue waveform) with a period determined mainly by the inductance of TR1 and capacitance of C. The same current also charges the capacitor C, and most importantly, injects charges into the P-N junction of the diode D. During this time, a linearly increasing current flows through the transistor T1 and the primary winding of the transformer (similarly to the flyback boost converter). The windings and core of the transformer should be selected so that the core saturates when the voltage peaks across the capacitor C (the violet waveform). That point in time occurs after half a period of the secondary circuit's oscillation. It is possible to make a simple test during the selection of the core and the making of the windings: Measure the primary current while the secondary winding is shorted (so that the resonating current does not influence the measurement). Beginning with short pulses, observe the current in the winding. A current waveform that curves up is an indication of core saturation (see Fig. 4). In the circuit presented here, the saturation begins when the T1 gate pulse width reaches approximately 160ns. This means, that for such a transformer, the half-period of the secondary circuit's oscillation should have this duration, too.



(a) (b)

Fig.4: (a) short conduction of the transistor does not saturate the core *(b) however a longer pulse (170ns) is already capable of causing the saturation. Both measurements were made with the secondary winding shorted. The yellow waveforms reflect the voltages on the gate of T1 and the blue waveforms reflect the currents flowing in the primary winding.*

The capacitor C begins to discharge, when the secondary current reverses (and it will reverse, according to the well known behavior of underdamped LC circuits). The saturation of the core is very important at this moment because it significantly decreases winding impedances (only the secondary winding is significant at this point) and it magnetically separates both windings. Due to this, the reverse current reaches much higher level than in the first half-period and its frequency increases, too. At the same time the space charge previously injected into the P-N junction of the diode D, is depleted. A this time, the diode is still forward biased and it presents a low impedance to the resonating current, because this diode recovers very slowly
(for the P600M, t_{rr} = 2.5us).
The complete depletion of the junction's charge results in an abrupt interruption of the secondary LC circuit. This is the key phenomenon occurring in the Drift Step Recovery Diode. The semiconductor junction acts as a charge-controlled circuit breaker. The transformer should be constructed in such manner, that the interruption of this circuit occurs during the maximum discharge current.
The higher the interrupted current, the higher the generated voltage of the output pulse.

The drain circuit of transistor T1 can be already opened, since the saturation of the core is no longer needed. In reality, the transistor can be turned off as soon as the secondary current crosses zero, since the recovery from saturation takes significant time and limits the pulse repetition rate.

Component Selection

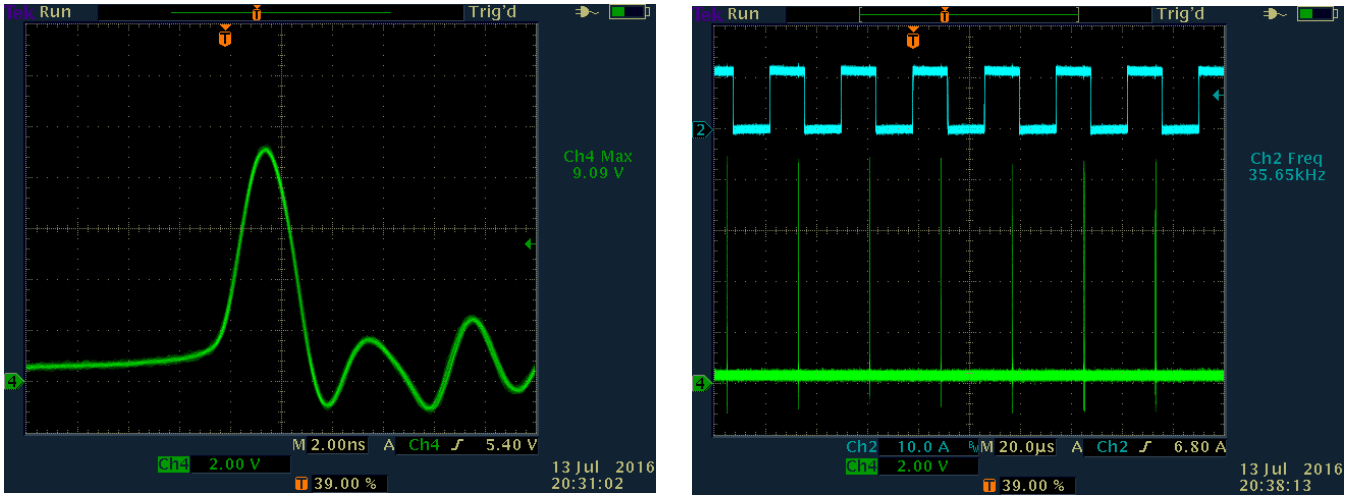
The transformer's core has to be small in order to saturate easily. Also, it should exhibit a high permeability so a small number of wire turns is sufficient to transfer the energy. Fewer turns result in a lower impedance of the secondary circuit after the core's saturation, which in turn allows a larger current to flow during the second half-period. The number of turns should be selected in such manner, that the transformer saturates when the voltage across capacitor C is at its maximum. The presented device used the core TN10/6/4-3E25 (made by Ferroxcube).
The windings were made with a 0.4mm Kynar wire and with the primary to secondary turn ratio of 6:12. The windings should be wound uniformly and cover the entire circumference of the core. It's worth to pay attention to the proper transformer's connections (there is an error in the publication [1] in the drawing 22). The diode D should be experimentally selected. This circuit performed well with slow rectifying diodes having large surface areas of the P-N junction and large reverse blocking voltage rating. The time t_{rr} must be significantly longer than the entire pulse cycle, so the P-N junction does not have the time to polarize and reverse block the discharge current.
Some Russian diodes described in the original publication [1] were tested. In the circuit researched herein, the selected diode P600M yielded pulses of higher voltage and steeper edges than USSR diodes mentioned in the original publication.

The capacitance of C influences the time constant and energy of the secondary LC circuit. A ceramic capacitor 2.2nF/10kV in parallel with 4.7nF/10kV was selected (6.9nF total).

The diode D2 suppresses high voltage transients on the drain of T1. A fast diode STTH8R06D, was selected.
The transistor T1 is a MOSFET with the V_{DS} >= 400V . A small gate charge allows for short gate pulse durations. The presented circuit also incorporates the MOSFET STW20NK50Z. A silicon carbide transistor (C3M0120090D) was also tested. This component indeed switched more efficiently and exhibited lower losses, but the cheap STW20NK50Z was used eventually, since the efficiency was not the goal of this implementation.
The transient voltage suppression diode D8 additionally protects the transistor T1. For this purpose, the 1.5KE440CA was selected because it featured a clamping voltage that is not much higher than the blocking voltage limit V_{DS} of T1.
The gate circuit is classic. It should allow for gate currents I_G > 4A. It is advantageous to accelerate the turning-off of the transistor T1 by diode D6. The driver TC4422 is capable of discharging the gate with a current of 10A. Its supply pins should be bypassed with fast ceramic capacitors > 1µF . The C4 capacitor should respond quickly. For this purpose a polypropylene capacitor FKP1G031005H00JSSD was used. All of the circuit's connections should be short since it is a high frequency circuit. The remaining components appearing on schematic in Fig.2 are not critical for the circuit's operation.

Peformance

The Fig.5a depicts the achieved pulse waveform shown with a timebase of 2ns/div. The pulses are measured by a self-made fast HV probe with attenuation of 1:250. Thus, a 9V pulse peak amplitude depicted on the scopeshot indicates the voltage of 2.25kV. The oscillations of the depicted pulse are a result of small probe impedance mismatch due to the probe's construction. The edges of the pulse last less than 2ns. The measurements were made with a fast oscilloscope Tektronix TDS3054C (500MHz, 5GS/s). The peak power in a 50Ω load reaches 100kW according to the relation P = U^2/R.
When supplied with 200VDC, this circuit works correctly up to approximately 50kHz of pulse repetition frequency. When loaded with 50Ω and supplied with 200VDC, the supply current is 90mA@16kHz and 215mA@36kHz. The Fig.5b depicts the generated pulses with the repetition frequency of 36kHz (the blue waveform is used for scope triggering).



(a) (b)

Fig.5: (a) *The achieved HV pulse measured with a 1:250 probe, (b) HV pulses repeated 35k times per second.*

Literature

[1] V.S. Belkin, G.I. Szułżenko,

ФОРМИРОВАТЕЛИ МОЩНЫХ НАНОСЕКУНДНЫХ И ПИКОСЕКУНДНЫХ ИМПУЛЬСОВ НА ПОЛУПРОВОДНИКОВОЙ ЭЛЕМЕНТНОЙ БАЗЕ

[2] V. Prokhorenko,
AN IMPULSE GENERATOR FOR THE GROUND PENETRATING RADAR