

C2M0025120D

Silicon Carbide Power MOSFET

C2M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Battery Chargers
- Motor Drive
- Pulsed Power Applications

Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

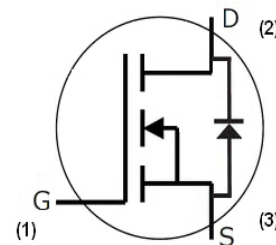
| Symbol | Parameter | Value | Unit | Test Conditions | Note |
|----------------|--|-------------|------------------|--|---------|
| V_{DSmax} | Drain - Source Voltage | 1200 | V | $V_{GS} = 0\text{ V}$, $I_D = 100\text{ }\mu\text{A}$ | |
| V_{GSmax} | Gate - Source Voltage | -10/+25 | V | Absolute maximum values | |
| V_{GSop} | Gate - Source Voltage | -5/+20 | V | Recommended operational values | |
| I_D | Continuous Drain Current | 90 | A | $V_{GS} = 20\text{ V}$, $T_C = 25^\circ\text{C}$ | Fig. 19 |
| | | 60 | | $V_{GS} = 20\text{ V}$, $T_C = 100^\circ\text{C}$ | |
| $I_{D(pulse)}$ | Pulsed Drain Current | 250 | A | Pulse width t_p limited by T_{jmax} | Fig. 22 |
| P_D | Power Dissipation | 463 | W | $T_c = 25^\circ\text{C}$, $T_J = 150^\circ\text{C}$ | Fig. 20 |
| T_J, T_{stg} | Operating Junction and Storage Temperature | -55 to +150 | $^\circ\text{C}$ | | |
| T_L | Solder Temperature | 260 | $^\circ\text{C}$ | 1.6mm (0.063") from case for 10s | |
| M_d | Mounting Torque | 1 8.8 | Nm lbf-in | M3 or 6-32 screw | |

| | |
|--------------------------|---------------|
| V_{DS} | 1200 V |
| $I_D @ 25^\circ\text{C}$ | 90 A |
| $R_{DS(on)}$ | 25 m Ω |

Package



TO-247-3



| Part Number | Package |
|-------------|----------|
| C2M0025120D | TO-247-3 |



Electrical Characteristics (T_c = 25 °C unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|----------------------|----------------------------------|------|------|------|------|--|------------|
| V _{(BR)DSS} | Drain-Source Breakdown Voltage | 1200 | | | V | V _{GS} = 0 V, I _D = 100 μA | |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | 2.6 | 4 | V | V _{DS} = V _{GS} , I _D = 15mA | Fig. 11 |
| | | | 2.1 | | V | V _{DS} = V _{GS} , I _D = 15mA, T _J = 150 °C | |
| I _{DSS} | Zero Gate Voltage Drain Current | | 2 | 100 | μA | V _{DS} = 1200 V, V _{GS} = 0 V | |
| I _{GSS} | Gate-Source Leakage Current | | | 600 | nA | V _{GS} = 20 V, V _{DS} = 0 V | |
| R _{DS(on)} | Drain-Source On-State Resistance | | 25 | 34 | mΩ | V _{GS} = 20 V, I _D = 50 A | Fig. 4,5,6 |
| | | | 43 | | | V _{GS} = 20 V, I _D = 50 A, T _J = 150 °C | |
| g _{fs} | Transconductance | | 23.6 | | S | V _{DS} = 20 V, I _{DS} = 50 A | Fig. 7 |
| | | | 21.7 | | | V _{DS} = 20 V, I _{DS} = 50 A, T _J = 150 °C | |
| C _{iss} | Input Capacitance | | 2788 | | pF | V _{GS} = 0 V | Fig. 17,18 |
| C _{oss} | Output Capacitance | | 220 | | | V _{DS} = 1000 V | |
| C _{rss} | Reverse Transfer Capacitance | | 15 | | | f = 1 MHz | |
| E _{oss} | C _{oss} Stored Energy | | 121 | | μJ | V _{AC} = 25 mV | Fig 16 |
| E _{AS} | Avalanche Energy, Single Pluse | | 3.5 | | J | I _D = 50A, V _{DD} = 50V | Fig. 29 |
| E _{ON} | Turn-On Switching Energy | | 1.4 | | mJ | V _{DS} = 800 V, V _{GS} = -5/20 V, I _D = 50A, R _{G(ext)} = 2.5Ω, L = 412 μH | Fig. 25 |
| E _{OFF} | Turn Off Switching Energy | | 0.3 | | | | |
| t _{d(on)} | Turn-On Delay Time | | 14 | | ns | V _{DD} = 800 V, V _{GS} = -5/20 V I _D = 50 A, R _{G(ext)} = 2.5 Ω, R _L = 16 Ω Timing relative to V _{DS} Per IEC60747-8-4 pg 83 | Fig. 27 |
| t _r | Rise Time | | 32 | | | | |
| t _{d(off)} | Turn-Off Delay Time | | 29 | | | | |
| t _f | Fall Time | | 28 | | | | |
| R _{G(int)} | Internal Gate Resistance | | 1.1 | | Ω | f = 1 MHz, V _{AC} = 25 mV, ESR of C _{iss} | |
| Q _{gs} | Gate to Source Charge | | 46 | | nC | V _{DS} = 800 V, V _{GS} = -5/20 V I _D = 50 A Per IEC60747-8-4 pg 83 | Fig. 12 |
| Q _{gd} | Gate to Drain Charge | | 50 | | | | |
| Q _g | Total Gate Charge | | 161 | | | | |

Reverse Diode Characteristics

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|------------------|----------------------------------|------|------|------|---|---------------|
| V _{SD} | Diode Forward Voltage | 3.3 | | V | V _{GS} = - 5 V, I _{SD} = 25 A | Fig. 8, 9, 10 |
| | | 3.1 | | V | V _{GS} = - 5 V, I _{SD} = 25 A, T _J = 150 °C | |
| I _S | Continuous Diode Forward Current | | 90 | | T _c = 25 °C | Note 1 |
| t _{rr} | Reverse Recovery Time | 45 | | ns | V _{GS} = - 5 V, I _{SD} = 50 A, T _J = 25 °C VR = 800 V dif/dt = 1000 A/μs | Note 1 |
| Q _{rr} | Reverse Recovery Charge | 406 | | nC | | |
| I _{rrm} | Peak Reverse Recovery Current | 13.5 | | A | | |

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|------------------|---|------|------|------|-----------------|---------|
| R _{θJC} | Thermal Resistance from Junction to Case | 0.24 | 0.27 | °C/W | | Fig. 21 |
| R _{θJA} | Thermal Resistance from Junction to Ambient | | 40 | | | |

Typical Performance

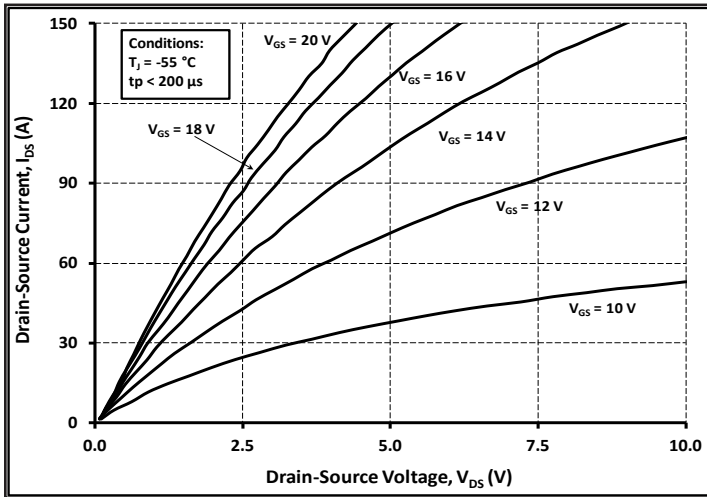


Figure 1. Output Characteristics $T_J = -55\text{ }^{\circ}\text{C}$

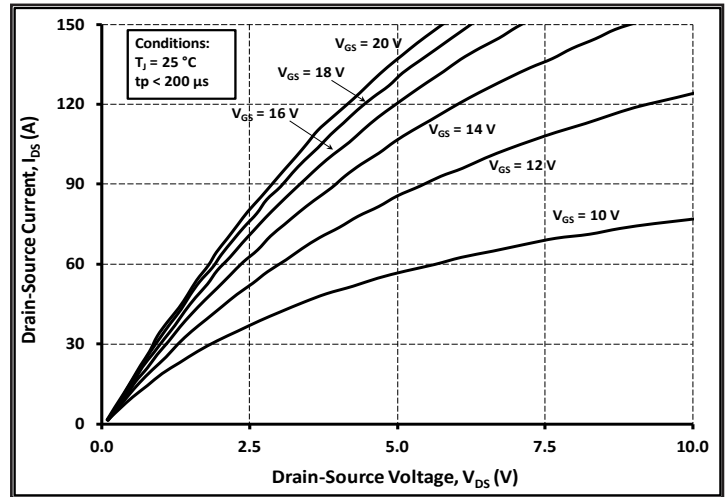


Figure 2. Output Characteristics $T_J = 25\text{ }^{\circ}\text{C}$

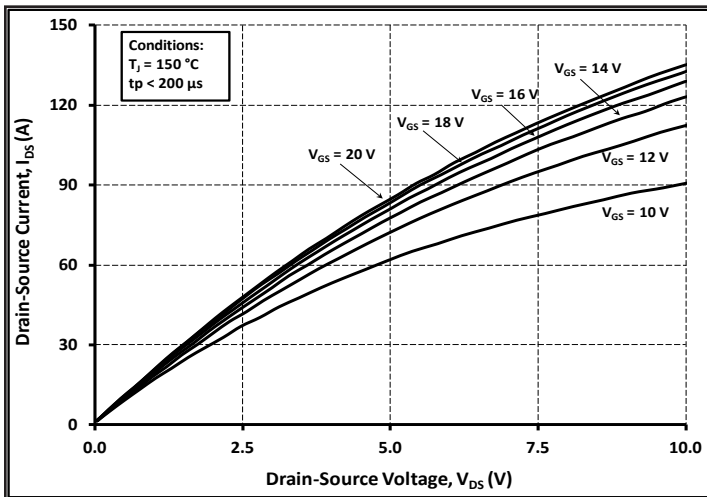


Figure 3. Output Characteristics $T_J = 150\text{ }^{\circ}\text{C}$

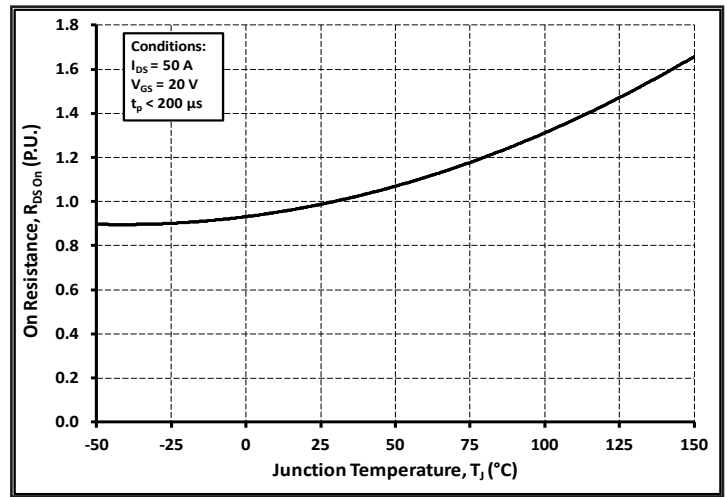


Figure 4. Normalized On-Resistance vs. Temperature

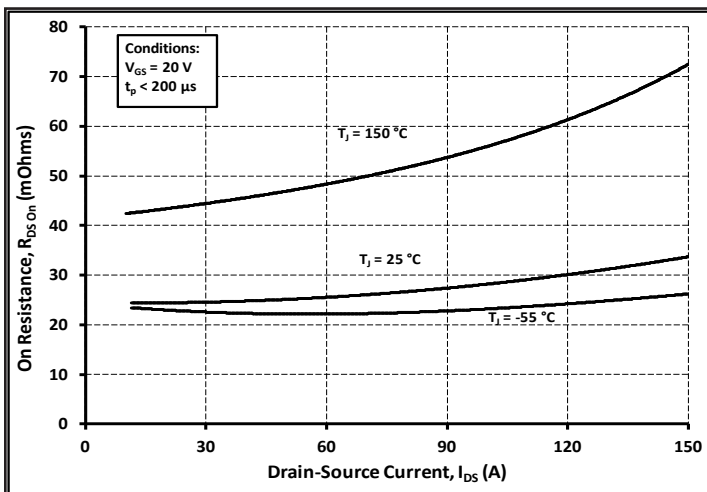


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

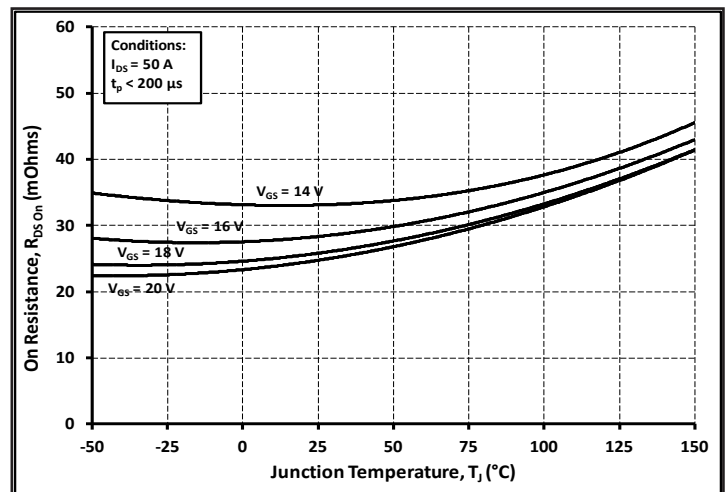


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

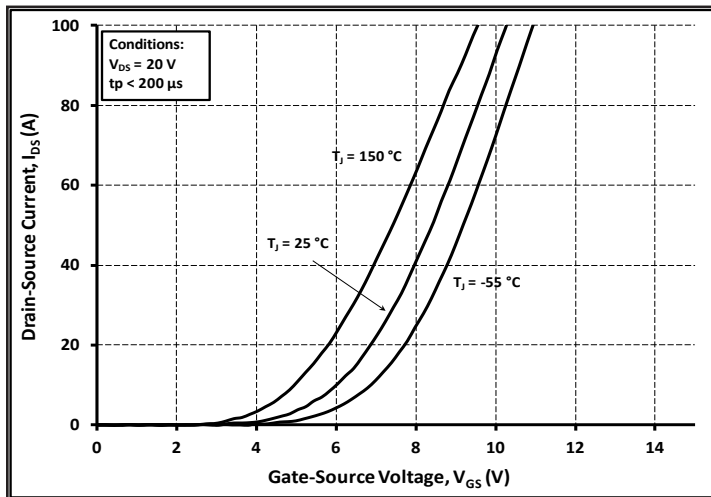


Figure 7. Transfer Characteristic For Various Junction Temperatures

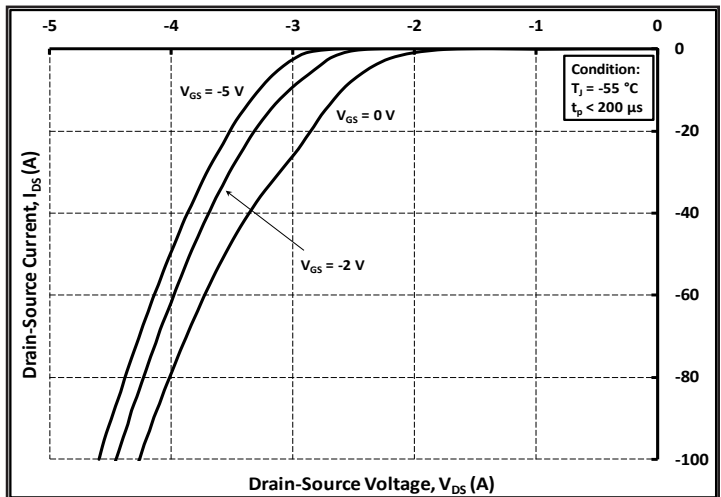


Figure 8. Body Diode Characteristic at $-55\text{ }^{\circ}\text{C}$

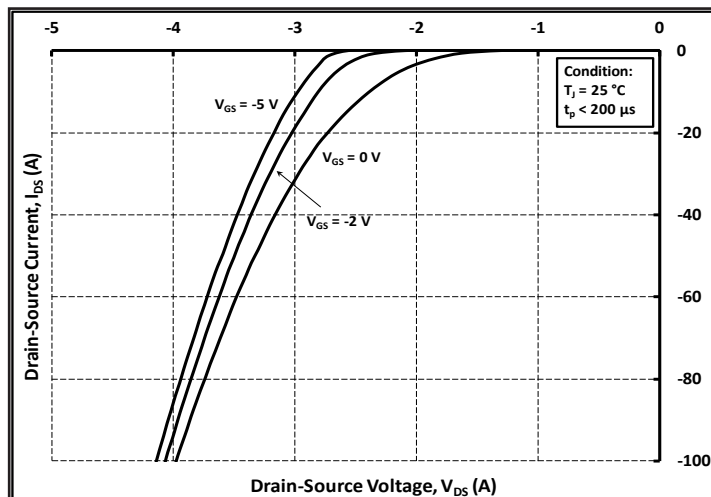


Figure 9. Body Diode Characteristic at $25\text{ }^{\circ}\text{C}$

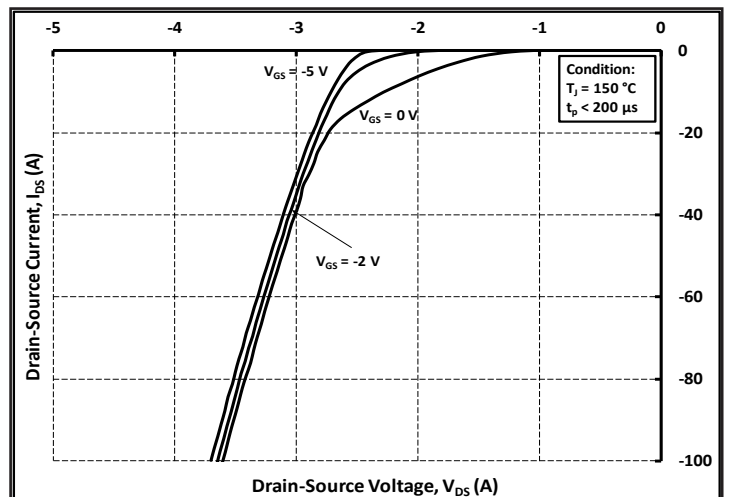


Figure 10. Body Diode Characteristic at $150\text{ }^{\circ}\text{C}$

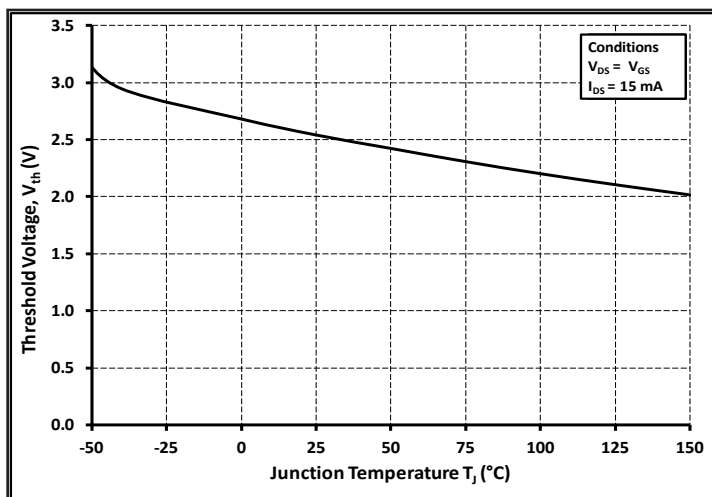


Figure 11. Threshold Voltage vs. Temperature

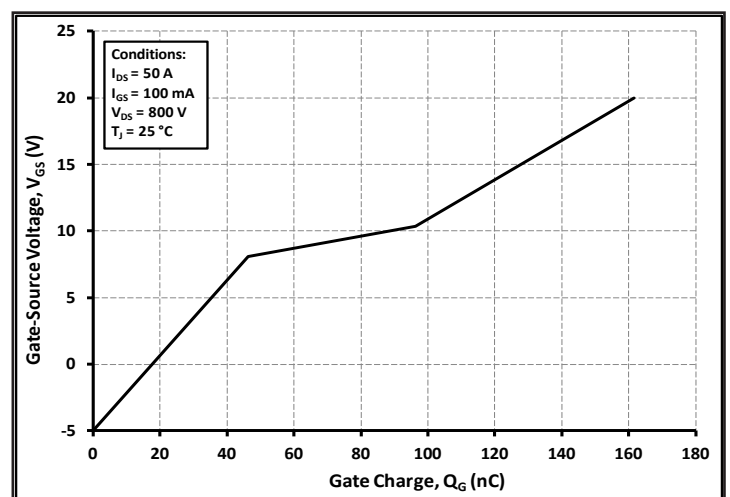


Figure 12. Gate Charge Characteristic

Typical Performance

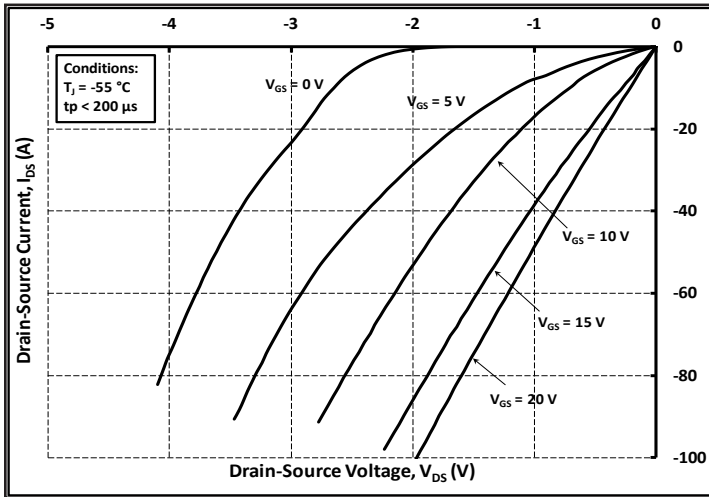


Figure 13. 3rd Quadrant Characteristic at -55 °C

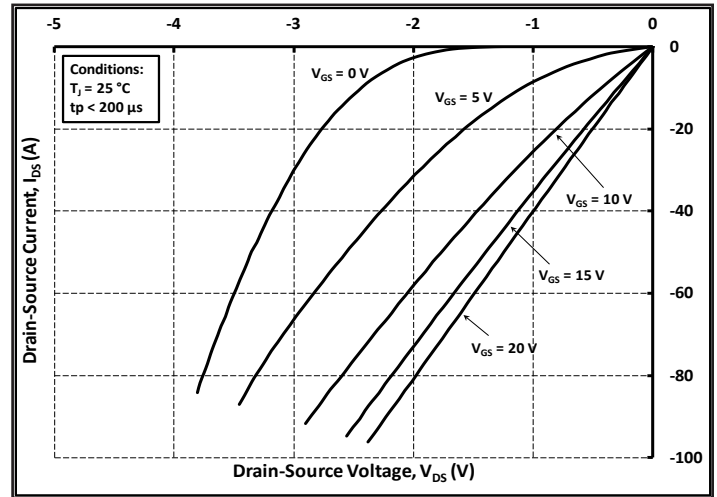


Figure 14. 3rd Quadrant Characteristic at 25 °C

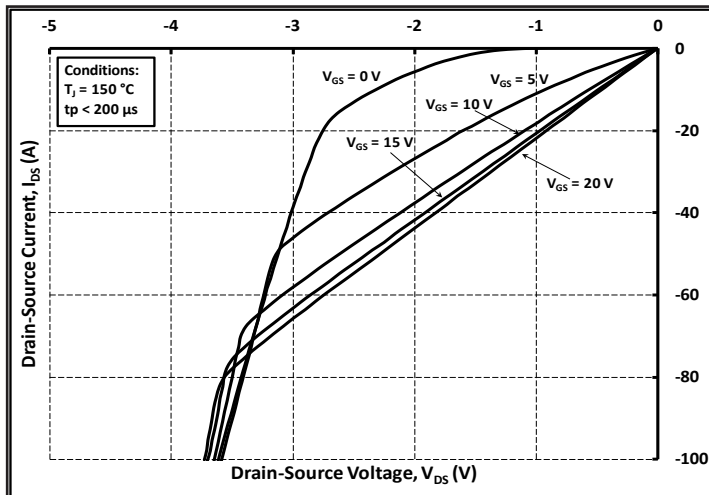


Figure 15. 3rd Quadrant Characteristic at 150 °C

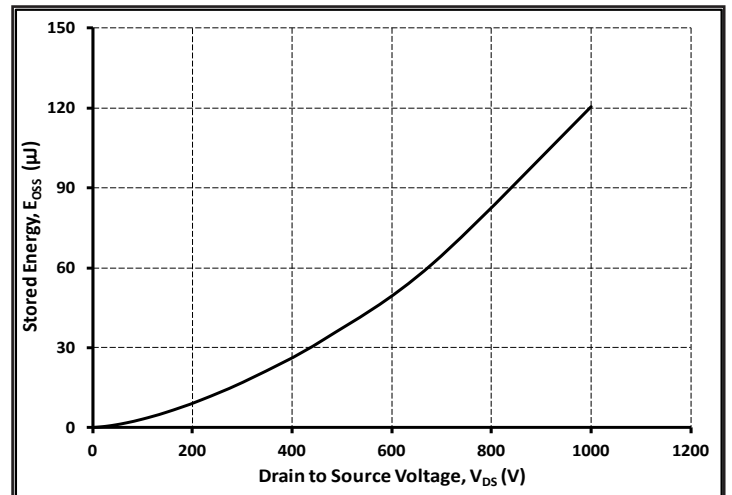


Figure 16. Output Capacitor Stored Energy

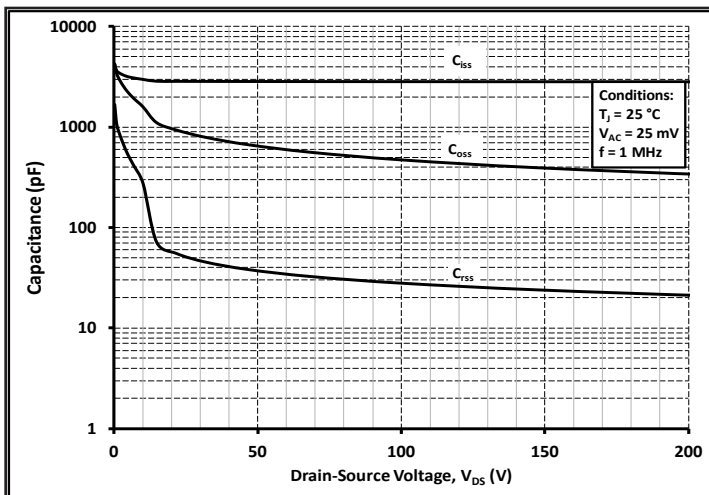


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

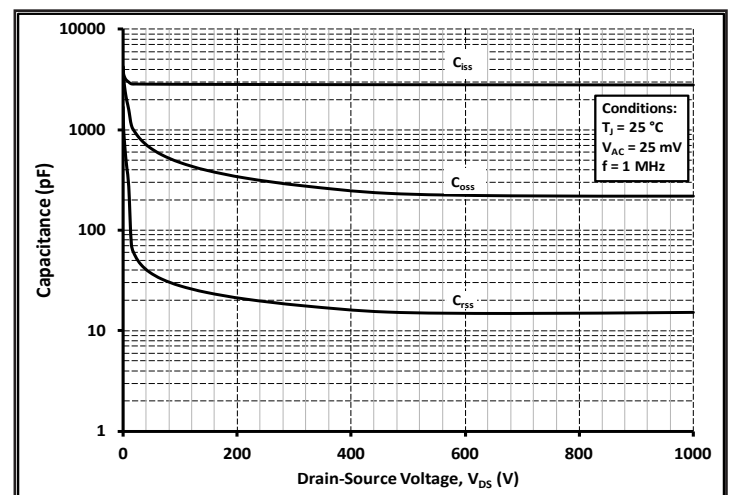


Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

Typical Performance

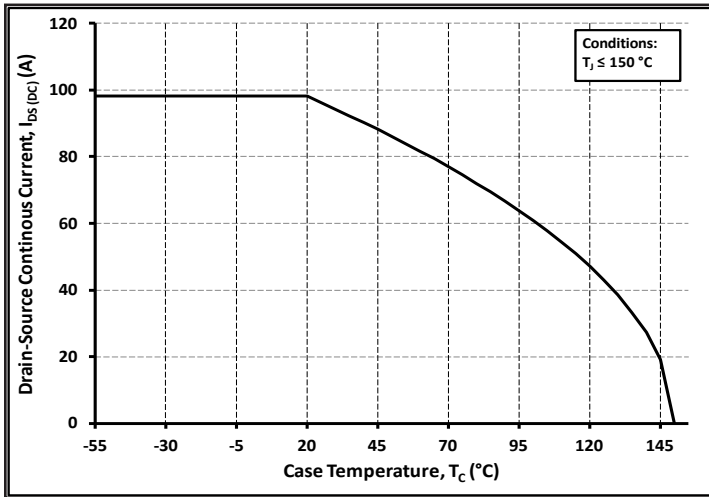


Figure 19. Continuous Drain Current Derating vs. Case Temperature

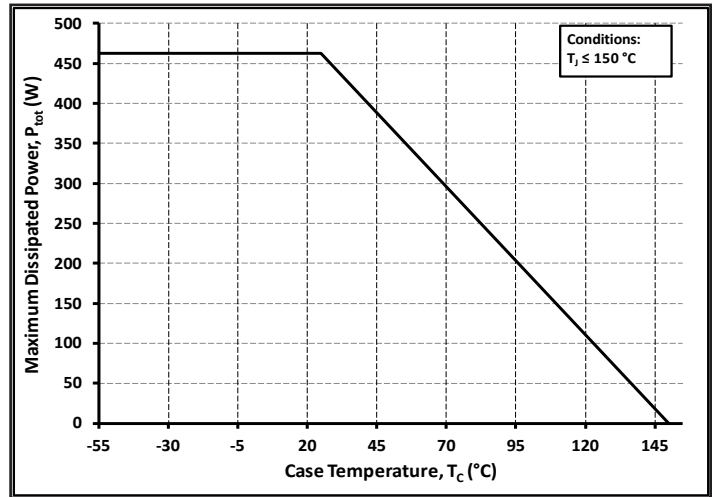


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

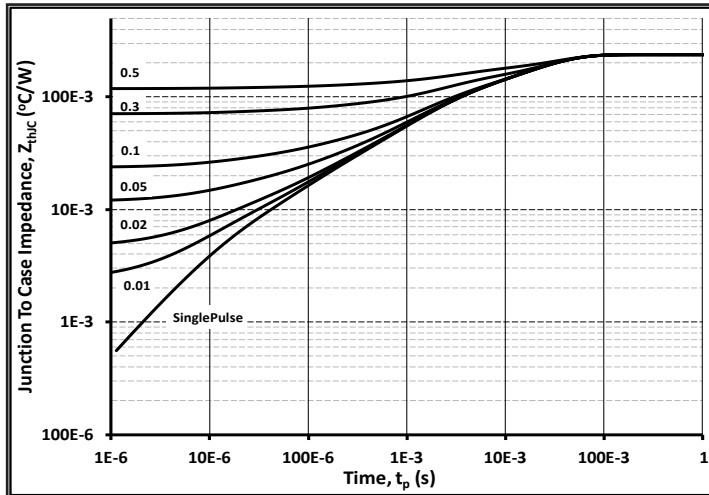


Figure 21. Transient Thermal Impedance (Junction - Case)

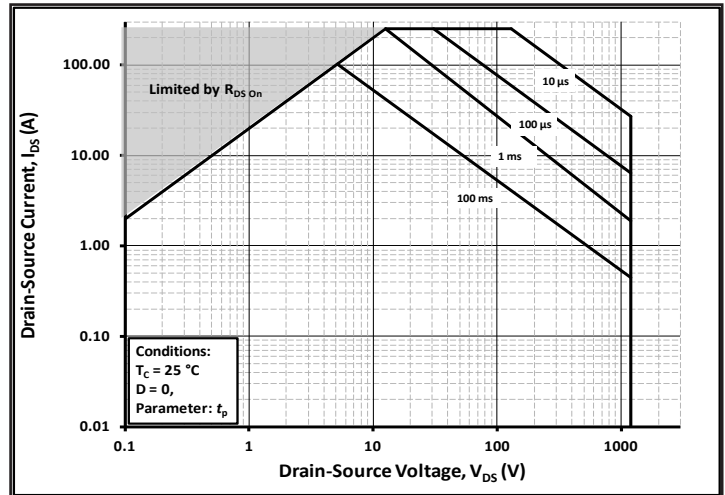


Figure 22. Safe Operating Area

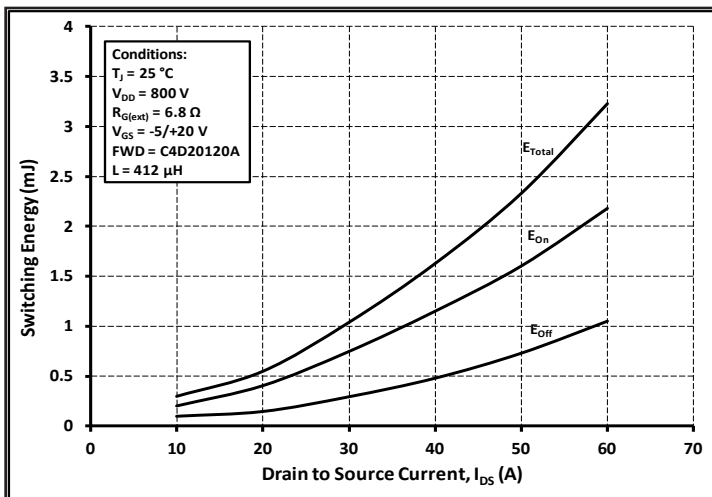


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800V$)

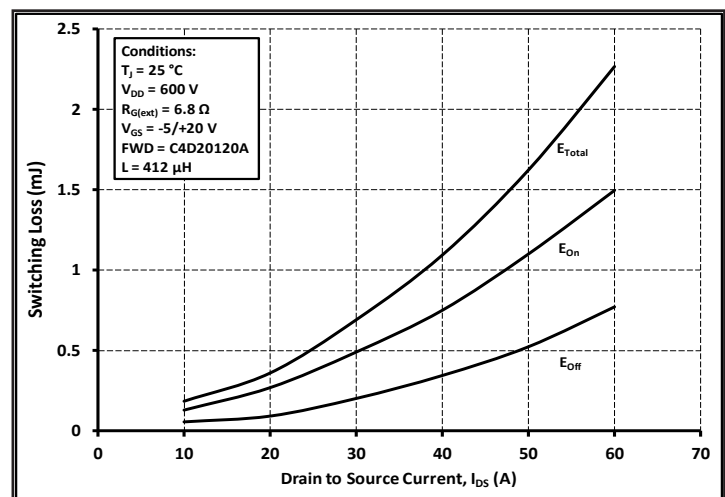


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600V$)

Typical Performance

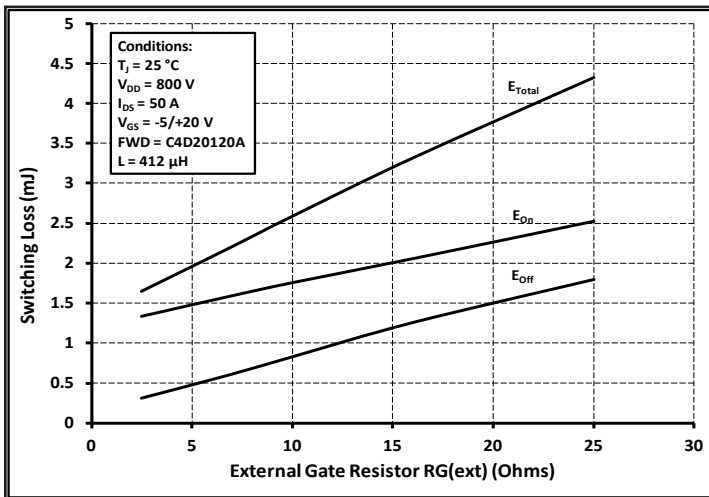


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(\text{ext})}$

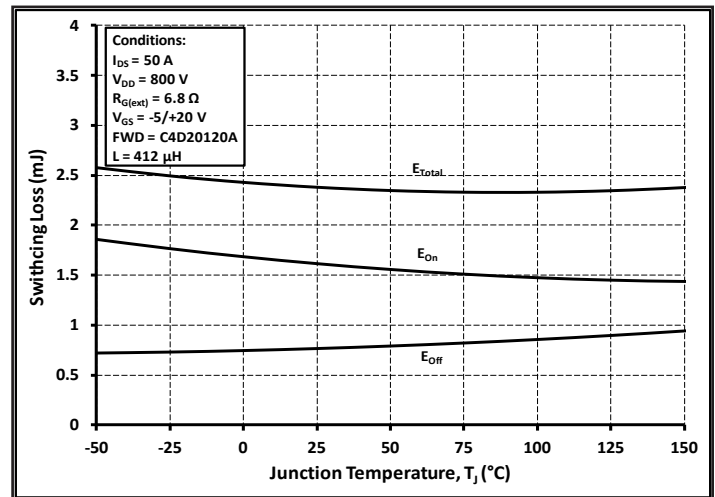


Figure 26. Clamped Inductive Switching Energy vs. Temperature

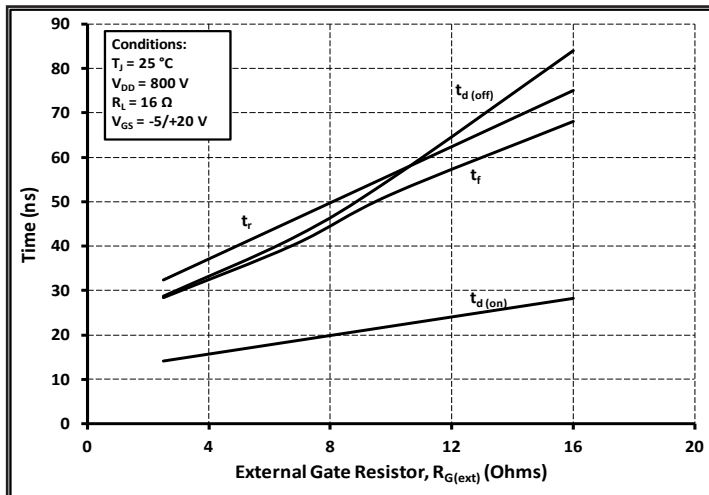


Figure 27. Switching Times vs. $R_{G(\text{ext})}$

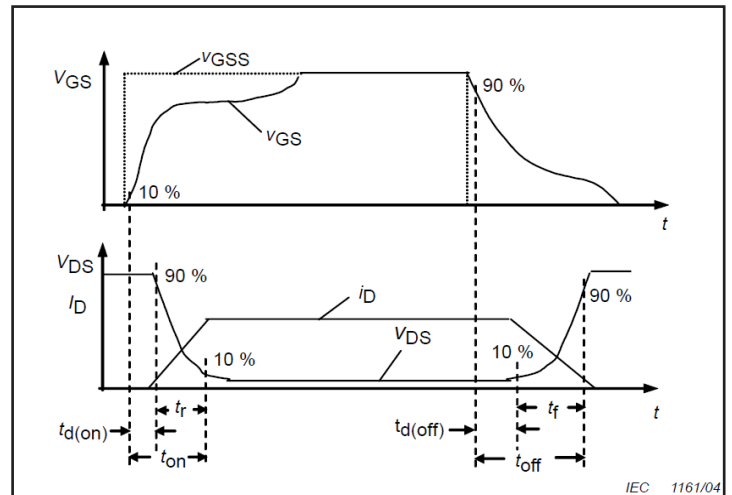


Figure 28. Switching Times Definition

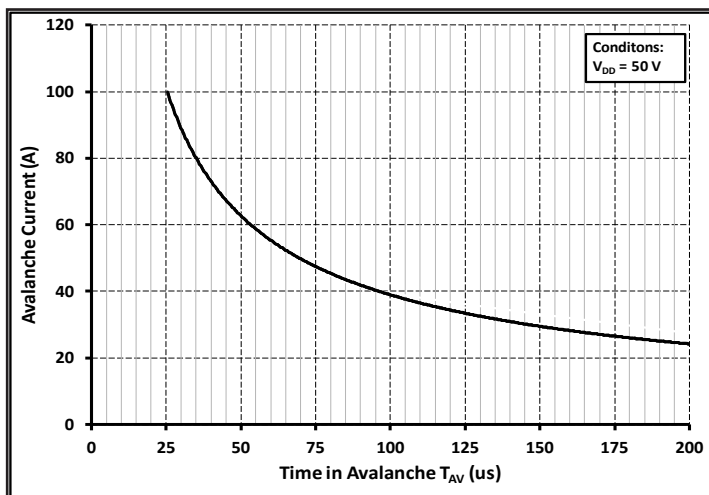


Figure 29. Single Avalanche SOA curve

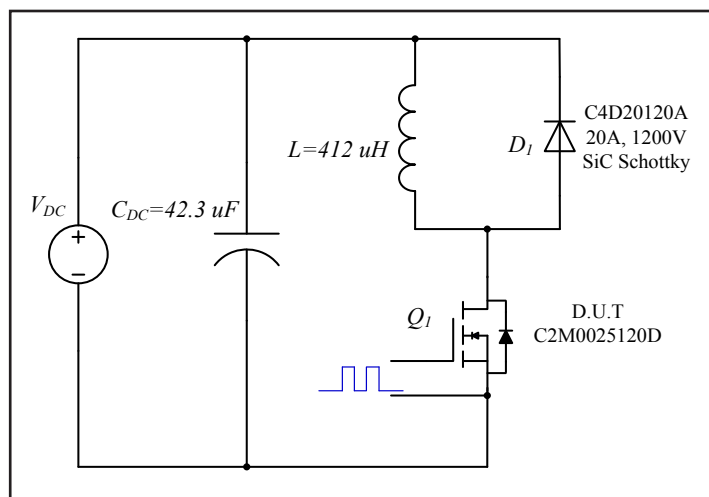


Figure 30. Clamped Inductive Switching Waveform Test Circuit

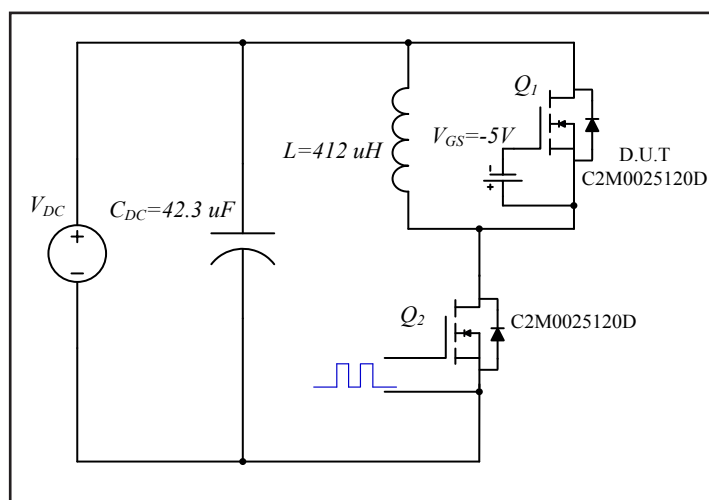


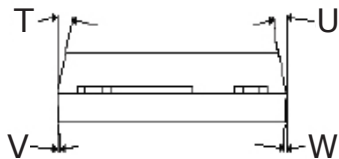
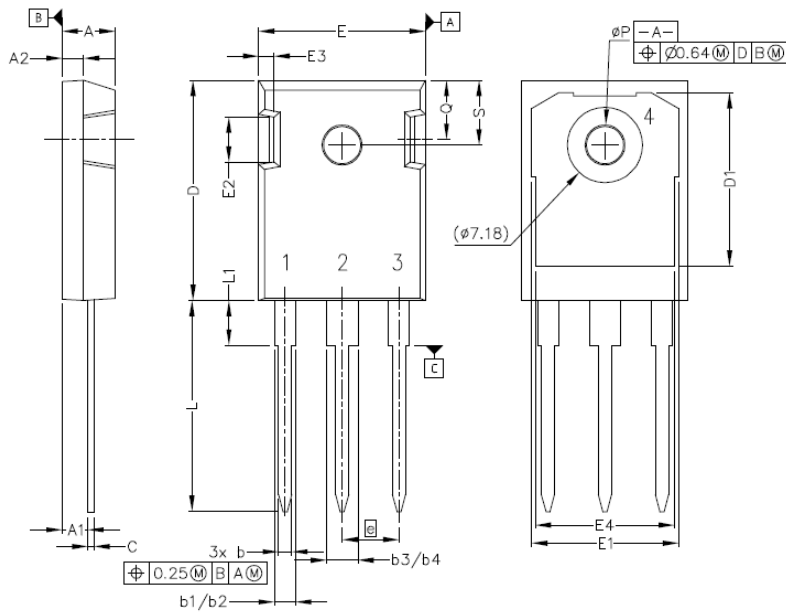
Figure 31. Body Diode Recovery Test Circuit

ESD Ratings

| ESD Test | Total Devices Sampled | Resulting Classification |
|----------|--------------------------|--------------------------|
| ESD-HBM | All Devices Passed 1000V | 2 (>2000V) |
| ESD-MM | All Devices Passed 400V | C (>400V) |
| ESD-CDM | All Devices Passed 1000V | IV (>1000V) |

Package Dimensions

Package TO-247-3

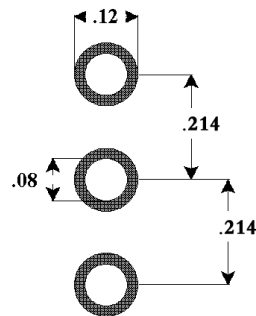


Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

| POS | Inches | | Millimeters | |
|-----|----------|------|-------------|-------|
| | Min | Max | Min | Max |
| A | .190 | .205 | 4.83 | 5.21 |
| A1 | .090 | .100 | 2.29 | 2.54 |
| A2 | .075 | .085 | 1.91 | 2.16 |
| b | .042 | .052 | 1.07 | 1.33 |
| b1 | .075 | .095 | 1.91 | 2.41 |
| b2 | .075 | .085 | 1.91 | 2.16 |
| b3 | .113 | .133 | 2.87 | 3.38 |
| b4 | .113 | .123 | 2.87 | 3.13 |
| c | .022 | .027 | 0.55 | 0.68 |
| D | .819 | .831 | 20.80 | 21.10 |
| D1 | .640 | .695 | 16.25 | 17.65 |
| D2 | .037 | .049 | 0.95 | 1.25 |
| E | .620 | .635 | 15.75 | 16.13 |
| E1 | .516 | .557 | 13.10 | 14.15 |
| E2 | .145 | .201 | 3.68 | 5.10 |
| E3 | .039 | .075 | 1.00 | 1.90 |
| E4 | .487 | .529 | 12.38 | 13.43 |
| e | .214 BSC | | 5.44 BSC | |
| N | 3 | | 3 | |
| L | .780 | .800 | 19.81 | 20.32 |
| L1 | .161 | .173 | 4.10 | 4.40 |
| ØP | .138 | .144 | 3.51 | 3.65 |
| Q | .216 | .236 | 5.49 | 6.00 |
| S | .238 | .248 | 6.04 | 6.30 |
| T | 9° | 11° | 9° | 11° |
| U | 9° | 11° | 9° | 11° |
| V | 2° | 8° | 2° | 8° |
| W | 2° | 8° | 2° | 8° |

Recommended Solder Pad Layout



TO-247-3

| Part Number | Package | Marking |
|-------------|----------|------------|
| C2M0025120D | TO-247-3 | C2M0025120 |



Notes

- **RoHS Compliance**
The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.
- **REACH Compliance**
REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a Cree representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.
- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **C2M PSICE Models:** <http://wolfspeed.com/power/tools-and-support>
- **SiC MOSFET Isolated Gate Driver reference design:** <http://wolfspeed.com/power/tools-and-support>
- **SiC MOSFET Evaluation Board:** <http://wolfspeed.com/power/tools-and-support>

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