Experimental Comparison of Low-Cost Sub-Nanosecond Pulse Generators

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***Abstract*—In this paper, six low-cost pulse generator devices having sub-nanosecond transition time are analyzed and compared. Some of the possible applications for these devices are also described, along with an overview of the different approaches for sub-nanosecond pulse generation. Furthermore, the architecture and principle of operation of the realized prototypes are explained. The considered pulse generation techniques are based on logic gates, Step-Recovery Diodes, and transistors driven in the avalanche region. Some experimental results obtained by using an equivalent-time sampling oscilloscope and a spectrum analyzer are shown and discussed, providing both a time-domain and a frequency-domain characterization of the prototypes. Finally, an approach for the generation of modulated pulses in the 6-GHz band (for ultra-wideband applications) is investigated, and experimental results are provided.**

***Index Terms*—Experimental characterization, pulse generation, pulse measurements, ultra-wideband signals.**

I. Introduction

SHORT-PULSE generation has applications in several areas, such as the following: 1) linear systems characterization; 2) time-domain reflectometry (TDR); and 3) ultra-wideband (UWB) systems. The characterization of linear systems relies substantially on the determination of their pulse response. Knowledge of an instrument's pulse response can be used to determine instrument performance and to compensate for non-ideal behaviors. As an example, the pulse response of a digital oscilloscope can be determined by measuring a properly-characterized fast pulse [1], having a much greater bandwidth than that of the oscilloscope under test. The measured spectrum contains harmonic sinusoidal components over the frequency range of interest (the oscilloscope's bandwidth). From the known pulse shape and the recorded oscilloscope response waveforms, the amplitude and phase of each Fourier harmonic component can be obtained using the Discrete Fourier Transform. Finally, the impulse response can be determined by the deconvolution of these two signals [2].

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Short pulse generators are commonly used in TDR systems to characterize long transmission lines and detect failures or potential problems. By analyzing pulse reflections, in fact, the impedance changes can be localized within the transmission line with high accuracy. This technique has also been applied to localize failures in printed circuit board traces or integrated circuit packages [3]. Short-pulse properties can also be exploited for material characterization [4], [5].

Another application area for fast-pulse generation is UWB systems, where sub-nanosecond pulse generation is one of the main issues. FCC First Report and Order of 2002 [6] defines an UWB system as any intentional radiator having a fractional bandwidth greater than 20% or an absolute bandwidth greater than 500 MHz. The origin of UWB technology dates back to the early 1960s within time-domain electromagnetics. After 45 years of technological advancement, UWB systems have been used in several application fields [7], such as:

- radar systems with high-range measurement accuracy and resolution;
- high-data rate, short-range communication systems;
- sensor networks for indoor geolocation;
- ground-penetrating radars.

UWB systems offer several advantages compared to traditional systems. First of all, they are a base-band technology; and consequently, an impulse-based UWB receiver does not need an intermediate frequency stage, thus, widely reducing system complexity and cost. Moreover, the signal power is spread over a wide range of frequencies, with an extremely low power spectral density. This ensures small interference to other narrow band radio frequency (RF) signals and maintains excellent immunity to interference from these signals. Therefore, UWB devices can work within frequency intervals allocated for other RF systems. This characteristic, along with their immunity to multipath phenomena, makes UWB signals good candidates for several indoor applications.

Among the short pulses, the monocycle pulse is of particular interest, since it presents a wideband spectrum without low-frequency and DC components, simplifying the design of various elements such as amplifiers and antennas [8]. Several approaches have been proposed to produce monocycle pulses [9]–[12]. In particular, the pulse-generating network can be realized with a full-custom approach based on CMOS technology, mainly for low-cost, low-power consumption, and easy integration in digital or mixed integrated circuits [9], [13]. This approach eases the implementation of tuning capabilities for the generation of pulses of different duration, that is a desirable function to allow range and resolution adjustments. More conventional approaches involve hybrid circuit techniques, with different pulse-generating network types. Many of these generators are based on a step recovery diode (SRD) [14]. The SRD can be used in series or shunt connection to speed up the input signal rise or fall time. In [10], the authors propose a tunable pulse generator based on a series SRD and parallel-connected PIN diodes alternated with a short-circuited stub. The number and length of the transmission line sections are chosen to obtain the desired number and duration of pulses. In [15], the authors implement a pulse-shaping network using a transmission line and a MESFET. This network converts an input voltage source into a current source, which drives the SRD and allows the pulse generation with very little distortion. Furthermore, the MESFET facilitates broadband matching to the transmission line due to a very large gate-source input impedance and allows the use of a high pulse repetition frequency. Another way to generate short pulses is based on the step recovery effect in bipolar RF transistors [16]. Compared to the SRD, the transistor offers several advantages. The three-terminal structure simplifies the isolation problem between input and output signals. Furthermore, its current gain can be used to minimize the power of the driving signal.

In [11], the authors propose a “logical pulser” circuit with commercial off-the-shelf components (an inverter and a NAND or XOR gate). The pulse width is determined by the inverter propagation delay, whereas, the pulse edge depends on the rise/fall time of the output stage. To provide the required pulse duration, ECL logic components have been used due to their very high speed. The logic gate switching approach for pulse generation is also adopted in [12], where an architecture based on ECL Flip/Flops and a local oscillator is presented. The pulse generator can also be realized using a transistor driven in avalanche mode [17].

The main contribution of this paper is a thorough experimental analysis of the performance of several pulse generation approaches. The context of this analysis is represented by the potential applications, some of which have been described above in this section. Therefore, this paper provides a comparison of laboratory acquisitions obtained from low-complexity and low-cost prototypes, realized with off-the-shelf components. Preliminary versions of some of these devices have been presented in [18]. The six realized prototypes are based respectively on:

- AHCMOS logic gates;
- ECL logic gates (two versions);
- SRD;
- bipolar transistor driven in avalanche mode;
- upconverting mixer approach.

This paper is organized as follows. Section II presents the principle of operation and detailed design information for the developed pulse generator devices. Section III shows some experimental results from the realized prototypes, characterized by means of an equivalent-time sampling oscilloscope and a spectrum analyzer. The procedure used for the metrological characterization of the realized devices is described in Section IV. Section V provides a discussion of the experimental results and Section VI reports conclusions.

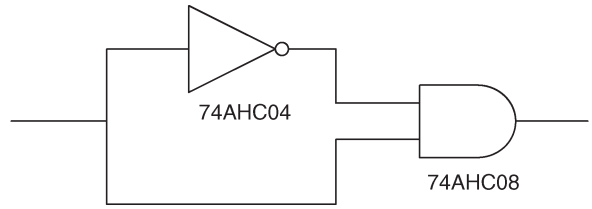

Fig. 1. Block diagram of the AHCMOS-based pulse generator.

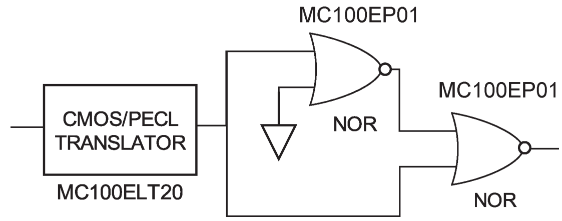

Fig. 2. Block diagram of the ECL-based pulse generator.

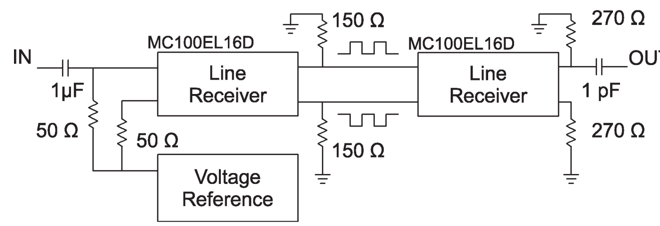

Fig. 3. Block diagram of the second ECL-based pulse generator.

II. Pulse Generators Design

The AHCMOS pulse generator consists of two logic gates connected as shown in Fig. 1. The circuit is designed to exploit the race condition at the output gate to generate a short glitch. Therefore, the pulse width mostly depends on the first gate propagation delay, whereas, its transition time is limited by the rise time of the output stage. The input waveform is split into two signals, each of them following a different path. The first path is directly connected to the AND gate input, whereas, the second goes to the inverter gate input. The propagation delay introduced by the inverter gate determines a skew of the AND gate inputs and allows the generation of the pulse. The AHCMOS logic family has been chosen for its low-current consumption and fast transition time. It can be noted that the performance cannot be improved using a following stage based on SRD, because the maximum output current of the AHCMOS family logic gates is not sufficient to permit the step recovery effect.

The first ECL pulse generator is obtained following a similar approach, and it is based on the circuit described in [11]. Fig. 2 shows the block diagram of the device. In this case, a level translator chip is used at the input to ensure level compatibility with a CMOS pulse trigger signal.

An additional ECL-based pulse generator has been developed, with a design based on the harmonic generator described in [19]. It is composed of a cascade of two differential line receivers, as shown in Fig. 3. The first stage is used to amplify the input signal to the positive-ECL logic levels, while the second

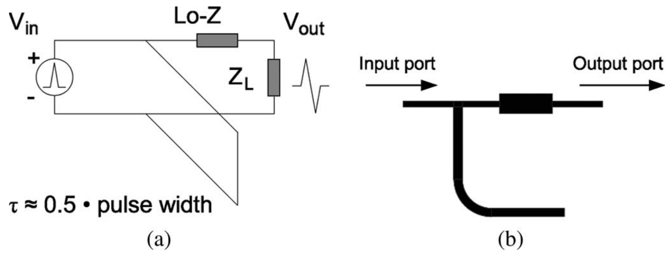

Fig. 4. (a) Schematic diagram of the planar monocycle pulse shaper. (b) Layout of the realized prototype.

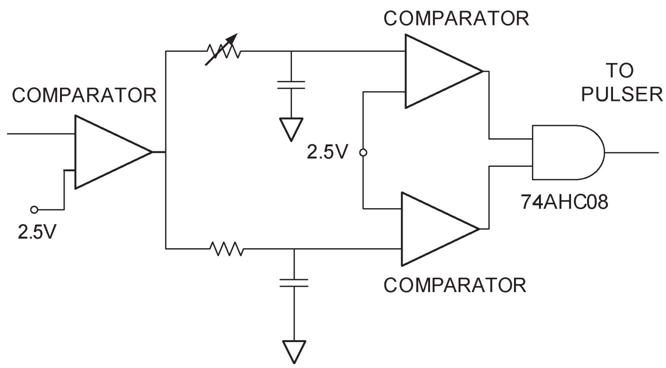

Fig. 5. Block diagram of the SRD-based pulse generator driver module.

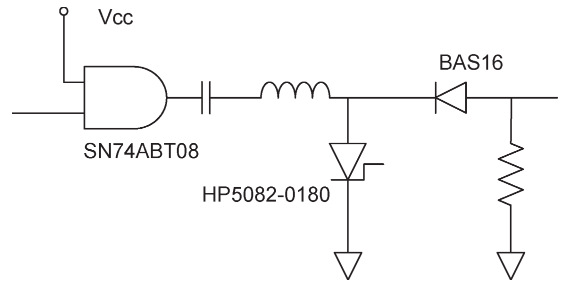

Fig. 6. Block diagram of the SRD-based pulser.

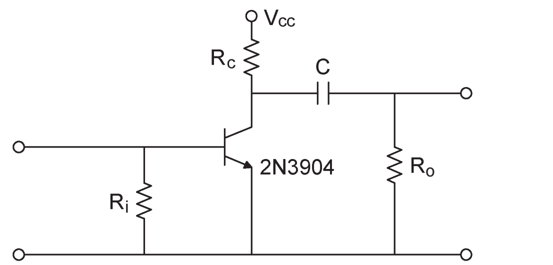

Fig. 7. Schematics of the pulse generator based on the avalanche transistor.

stage is driven into saturation, since its differential inputs are set to the full logic swing with opposite polarities. Therefore, when a sinusoidal input signal is connected, the output signal is a positive-ECL square wave with transition times of the order of a hundred picoseconds. The output 1 pF capacitor is used to differentiate this square wave signal, providing sub-nanosecond pulses. Since the square wave is characterized by both rising and falling edges, the resulting output pulses are alternatively positive and negative.

Furthermore, a monocycle-forming network has been realized, based on a short-circuited microstrip transmission line [20]. When connected to the output of the ECL pulse generator described above, this device provides a monocycle-type pulse shape. In particular, the short-circuited microstrip stub is designed to provide a delay equal to half the duration of the pulse provided by the second ECL generator. Therefore, the round-trip delay is equal to the total duration of the pulse. This allows the reflected pulse to sum with negative polarity and, thus, produce a monocycle waveform. Moreover, the series low-impedance transmission line section near the output connector has been introduced in order to improve impedance matching and reduce ringing. The network has been implemented in a standard double layer, 1.6-mm-thick, FR-4 substrate, with the schematic diagram and the layout shown in Fig. 4.

The SRD-based pulse generation device has been designed following a modular approach. Figs. 5 and 6 show the block diagram of the SRD driver and pulser modules, respectively. The driver module, based on the circuit described in [21], is designed to produce an adjustable-duration positive pulse when triggered by an input rising edge. The value of the variable resistor can be modified to obtain the desired duration of the output pulse waveform, which serves as the input for the SRD pulser. In this case, the duration has been set at approximately 100 ns. The SRD pulser circuit, shown in Fig. 6, features a BiCMOS logic buffer gate, chosen for its high-drive capability, which functions as a current driver. The output of this gate is connected to a pulse-shaping network and to the SRD. When forward-biased, this component stores charge, appearing as a low impedance device. During the reverse bias, the stored charge is removed by the reverse current. When all charge has been removed, an abrupt increment in the junction impedance occurs. This impedance transition can be exploited to generate very fast sub-nanosecond rise or fall times [14]. In this case, the shunt SRD provides a negative pulse on the falling edge of the input driving signal. The positive portion of this signal is then canceled by the clipping diode.

Fig. 7 shows the schematic of the pulse generator based on the avalanche transistor [17]. A DC feeding voltage of about 300 V allows the transistor to switch in avalanche mode, once a trigger pulse appears at the terminals of the input Base-Emitter resistor. When the transistor operates in the avalanche mode, an abrupt voltage drop at Collector-Emitter transistor junction appears and forces the output capacitor to discharge, resulting in a negative pulse at the output resistor terminals. The extremely low resistance of the transistor in avalanche mode results in a very short time constant of the capacitor discharge and, hence, in an extremely short fall time.

All pulse generators presented above have been designed for base-band operation. Additionally, a modulator prototype based on a voltage controlled oscillator (VCO) and on a mixer has been realized. Fig. 8 shows a block diagram of this circuit. The mixer is used to translate the input pulse spectrum around the local oscillator (LO) frequency of about 5.8 GHz, inside the boundaries defined by the FCC regulation. The base-band pulse is connected to the IF port of the mixer, while the modulated signal is present at the RF port.

III. Experimental Results

All the pulse generator prototypes have been realized as single-sided printed circuit boards using a standard

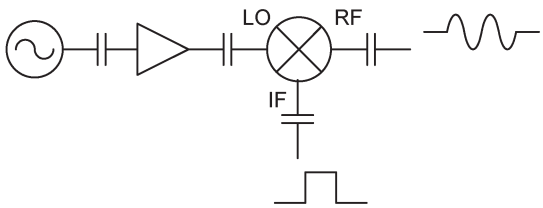

Fig. 8. Diagram of the modulator circuit: a 5.8-GHz VCO provides the carrier sinewave, which is then amplified and connected to the mixer LO port. The base-band pulse (generated by the AHC or ECL device) is connected to the mixer IF port, while the RF port provides the output modulated pulse.

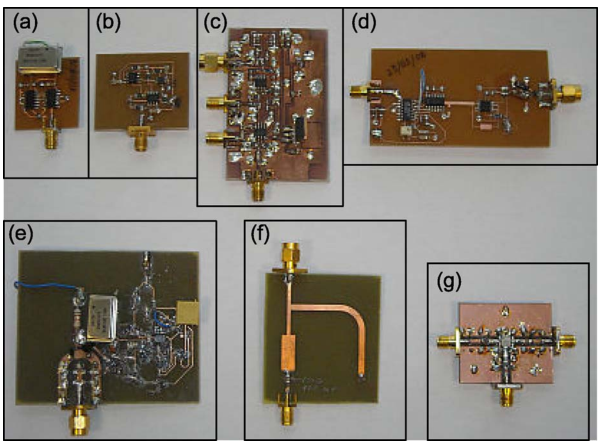

Fig. 9. Picture of the realized prototypes: (a) AHC, (b) first ECL, (c) second ECL, (d) SRD, (e) Avalanche, (f) Microstrip pulse shaper, (g) Mixer.

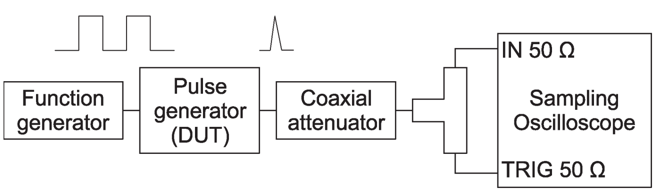

Fig. 10. Measurement setup, in the output triggering configuration.

1.6-mm-thick FR-4 Glass Epoxy substrate. Furthermore, a ground plane has been used to reduce the effects of interferences. Where available, surface mount components have been chosen, to minimize stray inductances. The width of the output trace has been calculated to obtain an output impedance of 50 Ω. Fig. 9 shows a picture of the realized prototypes.

The devices have been characterized using an equivalent-time sampling oscilloscope with an analog bandwidth of 20 GHz. Due to the maximum peak voltage specification of this instrument, some attenuators were used. However, the attenuation is compensated internally in the instrument. Furthermore, an external trigger signal was required by the sampling oscilloscope. In order to provide such a signal while minimizing the timing jitter, the measurement setup shown in Fig. 10 has been adopted. The pulse generator output port has been connected, by means of a coaxial T-connector, to the sampling input and to the trigger channel of the instrument, as shown in Fig. 10. It can be noticed that both channels are characterized by an input impedance of 50 Ω, therefore, the amplitude of the waveform shown by the instrument is relative to an impedance of 25 Ω. This measuring setup will be referred to as "output-triggering" in the following sections of this paper.

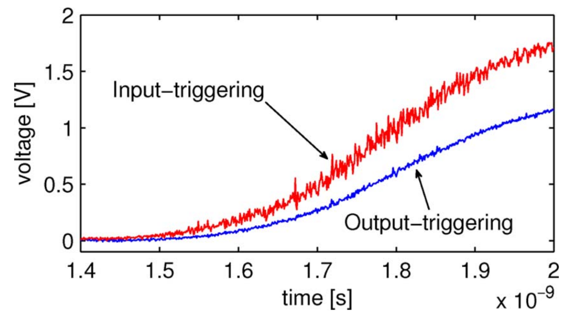

Fig. 11. Comparison between input-triggering and output-triggering configurations. It can be noticed that the waveform acquired with the output-triggering setup shows a decreased timing jitter and noise level.

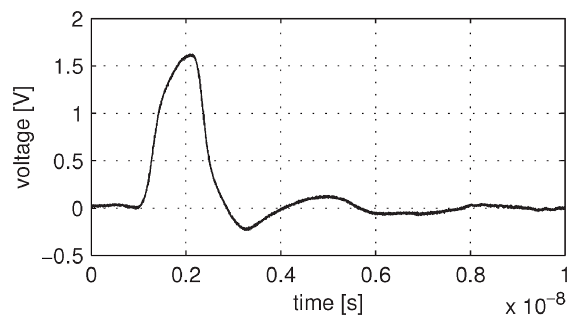

Fig. 12. AHC output acquired with 20-dB attenuation.

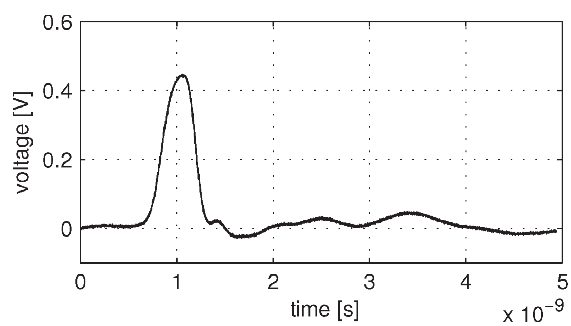

Fig. 13. ECL output acquired with 10-dB attenuation.

Initially, another measurement setup has been considered. Using this alternative setup, the input of the pulse generator is connected to the sampling oscilloscope trigger. This configuration has the drawback of increasing jitter, since the noise and timing jitter introduced by the pulse generator are visible in the acquired waveform. Therefore, this alternative setup, referred to as "input-triggering," has been discarded and the output-triggering configuration has been used for all the time-domain measurements described in this paper. A closeup of a rising-edge waveform by the same device acquired with the two different setups is shown for comparison in Fig. 11. The difference in voltage range is motivated by the different load impedance seen by the pulse generator in the two measurement setups.

Figs. 12–17 show the observed pulse generators waveforms. For the second ECL generator, results are also shown for the configuration using the pulse-shaping network (see Fig. 15).

To characterize the frequency-domain behavior of these pulse generators, their output power spectral density (PSD)

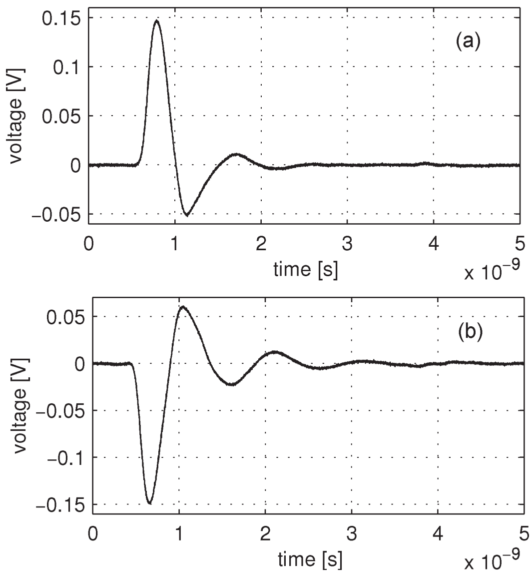

Fig. 14. Second ECL pulser (a) positive pulse and (b) negative pulse.

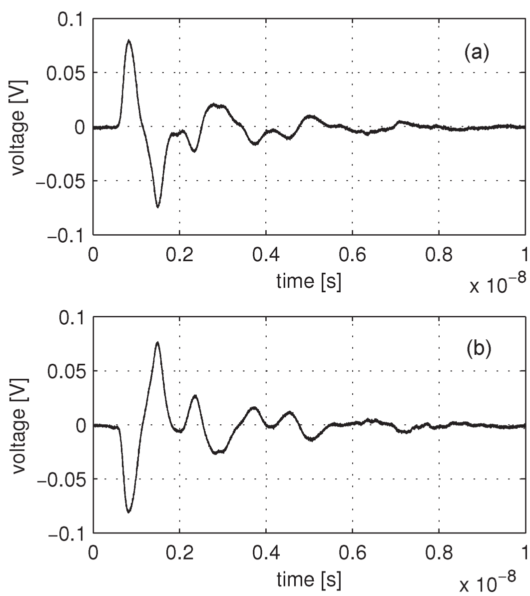

Fig. 15. Second ECL pulser, with pulse shaping applied on the (a) positive pulse and on the (b) negative pulse.

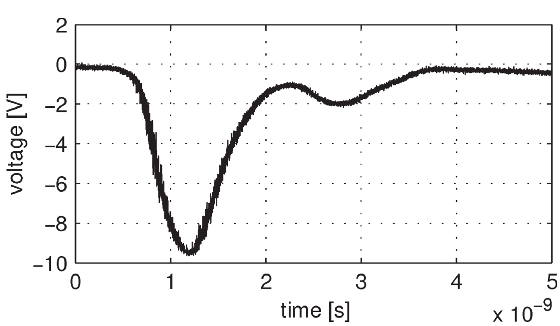

Fig. 16. SRD output acquired with 40-dB attenuation.

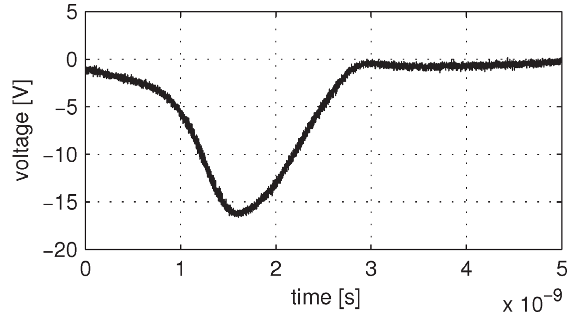

Fig. 17. Avalanche pulser output acquired with 50-dB attenuation.

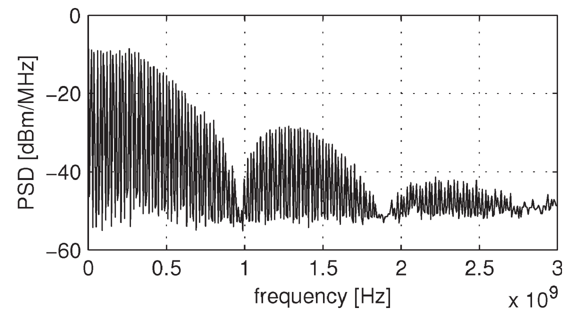

Fig. 18. AHC pulser PSD, 10-dB attenuation (1-MHz resolution bandwidth, 20-MHz pulse repetition frequency). A −10-dB bandwidth of about 700 MHz has been observed. Furthermore, the first zero of the spectrum is at about 1 GHz.

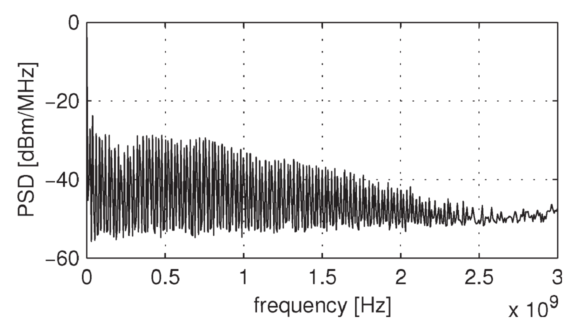

Fig. 19. First ECL pulser PSD, 10-dB attenuation (1-MHz resolution bandwidth, 20-MHz pulse repetition frequency). A −10-dB bandwidth of about 1.3 GHz has been observed, while the first zero is at about 2.5 GHz.

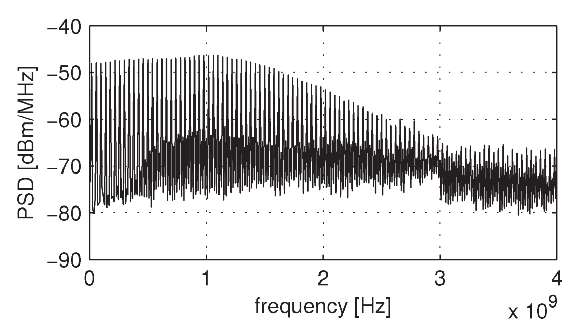

Fig. 20. Second ECL pulser PSD, 10 dB attenuation (1 MHz resolution bandwidth, 20 MHz pulse repetition frequency). A −10 dB bandwidth of about 2.2 GHz has been observed.

has been measured by means of a 9 kHz–26.5 GHz spectrum analyzer. Figs. 18–21 show the measured output PSD of the AHC and ECL pulse generators. The PSD was obtained with a pulse repetition frequency of 20 MHz and 1 MHz resolution bandwidth. Furthermore, the measured PSD for the SRD pulse generator is shown in Fig. 22. Due to the limitation on the repetition rate, in this case, the PSD was obtained with a pulse repetition rate of 2 MHz. To avoid damaging the instrument, the avalanche pulser was not connected directly to the spectrum analyzer. Instead, a spectral characterization has been performed

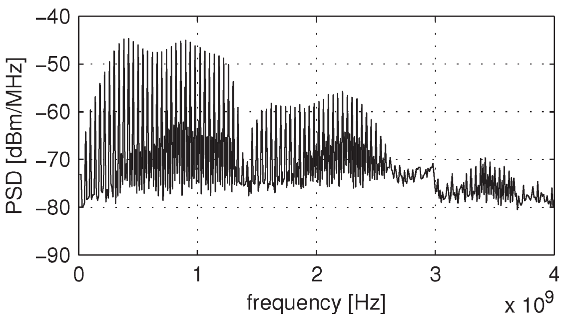

Fig. 21. Second ECL pulser with shaping network PSD, 10 dB attenuation (1 MHz resolution bandwidth, 20 MHz pulse repetition frequency). A −10 dB bandwidth of about 1 GHz has been observed, while the first zero is at about 1.5 GHz.

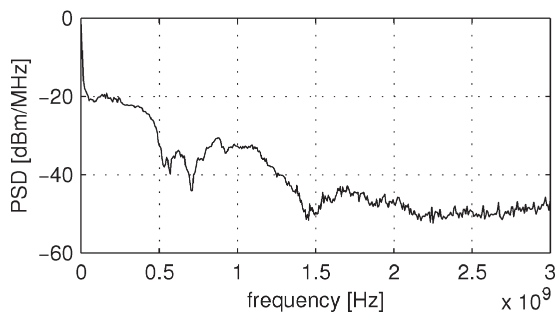

Fig. 22. SRD pulser PSD, 10-dB attenuation (1-MHz resolution bandwidth, 2-MHz pulse repetition frequency). A −10-dB bandwidth of about 500 MHz has been observed.

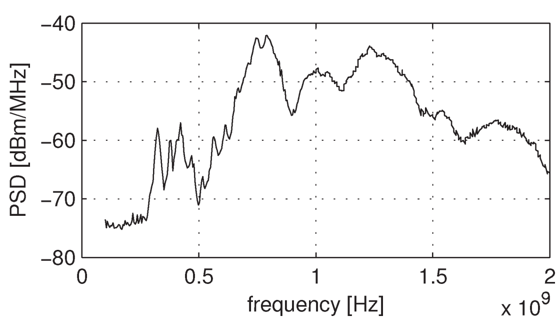

Fig. 23. Avalanche pulser radiated PSD (3-MHz resolution bandwidth, 100-kHz pulse repetition frequency).

by means of antennas. A wide band omnidirectional disc cone antenna was employed to transmit the pulse, while a receiving directional ridged-horn antenna was connected to the spectrum analyzer. The obtained trace is shown in Fig. 23.

The sampling oscilloscope acquisition shown in Fig. 24 is relative to the upconverting modulator applied to the AHC pulse generator, while Fig. 25 shows the measured output PSD with 20-MHz pulse repetition frequency and 1-MHz resolution bandwidth. Similarly, the acquisitions relative to the second ECL pulser are displayed in Figs. 26 and 27.

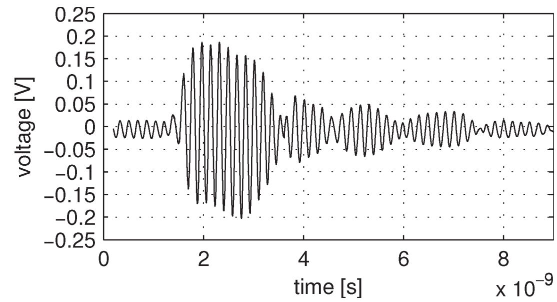

Fig. 24. Modulated AHC pulse.

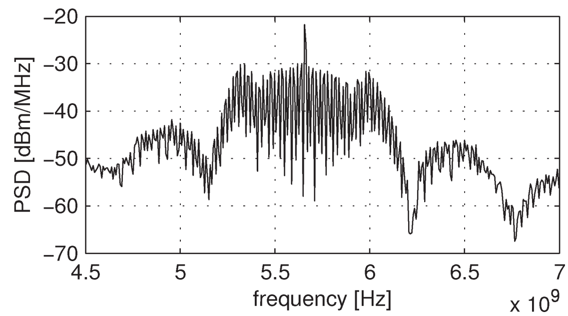

Fig. 25. PSD of the AHC pulser output mixed with the 5.8-GHz carrier (1-MHz resolution bandwidth, 20-MHz pulse repetition frequency). The observed main lobe width, between the first zeros of the spectrum, is approximately 1 GHz.

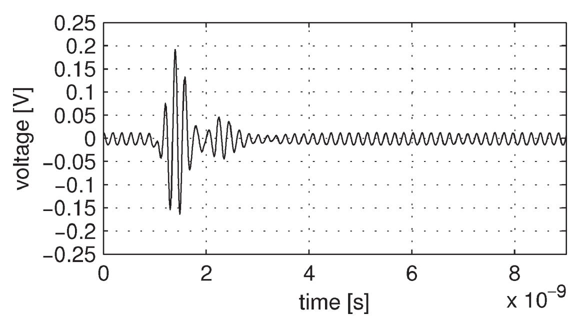

Fig. 26. Modulated second ECL pulse.

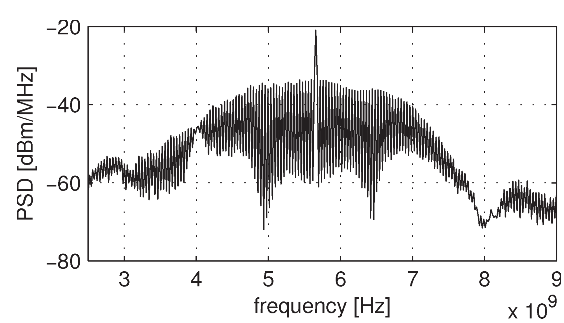

Fig. 27. PSD of the second ECL pulser output mixed with the 5.8-GHz carrier (1-MHz resolution bandwidth, 20-MHz pulse repetition frequency). The observed main lobe width, between the first zeros of the spectrum, is approximately 5 GHz, while the −10-dB bandwidth is about 3 GHz.

IV. Metrological Characterization

For each pulse generator, four parameters have been considered: 1) rise time (t_R); 2) fall time (t_F); 3) pulse width (t_W); and 4) peak-to-peak amplitude ($V_{\rm pp}$). Using the notation and guidance provided by the Guide to the Expression of Uncertainty in Measurement (GUM) [22], the Type A component of the standard uncertainty is evaluated by performing the statistical analysis of a series of repeated observations. Therefore, in this paper, it has been obtained by calculating the

TABLE I
TIME-DOMAIN CHARACTERIZATION SUMMARY

		AHC	first ECL	second ECL (positive)	second ECL (negative)	SRD	Avalanche
t_R	Measured value $[ps]$	594	220	122	168	678	796
	$u_A\,[ps]$	4.8	3.1	2.1	1.9	16	30
	$u_B\,[ps]$	0.9	0.7	0.6	0.7	0.9	1.0
	$u_C\,[ps]$	4.9	3.2	2.2	2.1	16	30
	$U_C\,[ps]$	14.7	9.6	6.6	6.3	48	90
t_F	Measured value $[ps]$	434	155	151	117	301	825
	$u_A\,[ps]$	4.2	2.8	1.9	1.9	13	38
	$u_B\,[ps]$	0.8	0.7	0.7	0.6	0.7	1.0
	$u_C\,[ps]$	4.3	2.9	2.1	2.0	13	38
	$U_C\,[ps]$	12.9	8.7	6.3	6.0	39	114
t_W	Measured value $[ps]$	1042	364	236	245	714	928
	$u_A\,[ps]$	1.0	2.3	0.9	0.7	14	19
	$u_B\,[ps]$	1.6	0.8	0.7	0.7	1.0	1.1
	$u_C\,[ps]$	1.9	2.4	1.1	1.0	14	19
	$U_C\,[ps]$	5.7	7.2	3.3	3.0	42	57
V_{pp}	Measured value $[V]$	1.9	0.49	0.199	0.211	9.6	17
	$u_A\,[V]$	0.0036	0.0011	0.0042	0.0004	0.033	0.32
	$u_B\,[V]$	0.078	0.020	0.0011	0.0012	0.55	1.2
	$u_C\,[V]$	0.078	0.020	0.0043	0.0013	0.55	1.2
	$U_C\,[V]$	0.234	0.060	0.0129	0.0039	1.65	3.6

TABLE II
FREQUENCY-DOMAIN CHARACTERIZATION SUMMARY

	AHC	first ECL	second ECL	second ECL (with pulse shaping)	SRD	Avalanche	AHC (with mixer)	second ECL (with mixer)
PSD Figure number	18	19	20	21	22	23	25	27
10-dB-bandwidth $[MHz]$	580	1700	2260	1150	490	760	890	3020
$u_C\,[MHz]$	17	17	23	46	17	23	35	92
$U_C\,[MHz]$	51	51	69	138	51	69	105	276

standard deviation of 1000 sampling oscilloscope observations, and is denoted as u_A.

Furthermore, a Type B evaluation of uncertainty has been performed, by taking into account the instrument specifications. From the sampling oscilloscope data sheet [23], the following accuracy specifications are obtained:

- Time Interval Accuracy: ± 1 ps $\pm 0.1\%$ of reading
- DC Vertical Voltage Accuracy: $< 1\%$ (800 mV_{pp} signal).

Assuming a uniform probability distribution of values inside the bounds provided by the instrument specifications, if the difference between the two bounds is denoted by 2Δ, then the Type B uncertainty component (denoted as u_B) is obtained as $\Delta/\sqrt{3}$. The tolerances of the coaxial attenuators, which were used, have also been taken into account in the evaluation of the Type B uncertainty. The specifications for the particular attenuator models used, of the BW-SXXW2+ series, have been obtained from the manufacturer's Web site.

Table I provides a summary of the time-domain characterization results, with the transition time, pulse width, and amplitude values measured by the instrument and the corresponding values of the Type A, Type B, and combined uncertainty u_C. The table includes also the combined expanded uncertainty U_C, evaluated with a coverage factor equal to three.

Although the main focus of this paper is on the time-domain metrological characterization, the uncertainty associated to the frequency-domain results has also been evaluated. The uncertainty values, calculated according to the spectrum analyzer data sheet [24], are summarized in Table II.

V. DISCUSSION

The experimental results presented in Table I show that the realized prototypes are capable of generating sub-nanosecond pulses. Furthermore, the metrological evaluation allowed to assess the good repeatability of the generated signals. By comparing the results of this extensive evaluation, it is possible to analyze several tradeoffs for the performances of the devices. In particular, the avalanche generator allows the generation of very fast and potentially high amplitude pulses, but it has limited Pulse Repetition Frequency (PRF) and it requires a high DC feeding voltage (300 V). These characteristics cause some implementation issues for many mobile applications. On the other hand, the AHC logical pulser features very low current consumption and potentially high PRF, but relatively slow transitions. Both the ECL-based designs produce a much faster rise time while requiring more current. Their output signals must be amplified to fulfill the requirements of some applications. Finally, the SRD-based circuit provides a good tradeoff between pulse performance and current consumption, but it is more complex, because it requires a proper driving network.

As shown by the results in Figs. 24–27, the pulse modulator prototype provides an effective means of translating the pulse spectrum in the UWB FCC band. However, significant carrier leakage is present, as shown by both time-domain and frequency-domain results. This is mainly due to isolation issues related to the mixer and the test fixture employed. Moreover, it can be noticed that the shorter pulse generated by the second ECL circuit provides a relatively smoother and wider spectrum with respect to the AHC device. However, due to requirements for the driving network, its minimum repetition rate is about 20 MHz, which could limit its application fields, while the AHC device has no such limitations. Only the second ECL and the AHC devices have been used with the modulator prototype, mainly due to pulse shape and power level considerations.

It is worthy of notice that in the literature, there are many examples of works aimed at realizing sub-nanosecond pulse generators. However, a significant number of these works deals with integrated circuit implementation, particularly in CMOS technology [13], [25]. These solutions allow to obtain many relevant features, such as reduced power consumption, pulse shape optimization, economy of scale, and improved overall performance. Our approach is characterized by a different aim, that is to realize simple low-cost pulsers with commercial off-the-shelf components, in order to enable quick experimentation with prototypes in a research lab environment.

VI. Conclusion

In this paper, experimental results obtained from six pulse generator prototypes are shown, and details on the architecture, and design issues are presented. The devices have been realized using commercially available off-the-shelf components in order to perform an analysis and comparison of several strategies for low-cost sub-nanosecond pulse generation. Results of a metrological characterization are discussed by evaluating the main advantages and drawbacks of each approach. In addition to the base-band pulse generators, an experimental analysis of the application of a modulation approach has been presented.

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