Steven Mark's

Toroidal Power Unit (TPU)

TP600 - TPU PULSER

- *A useful tool for TPU and other research*

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PREFACE

After folks have read through the SM material and feel they are ready to begin experimenting with ideas, one “must have” tool they need is a unit that can be used to pulse their coils.

It is the aim of this document to provide the design for such a tool. Keep in mind that the TP600 is for pulsing 3 coils only. It was not intended to pulse multiple coils in a sequence fashion….that would be another design project. For now though, the TP600 provides for 3 separate and independently controlled square wave generators, capable of frequencies from 0.4 Hz up to about 13 MHz. In addition, by changing the mode switch over to “SYNCHRONIZED”, the 3 outputs are harmonically related, and synchronized in time.

The design is by no means perfect or without the possibility of improvement, but as shown, should provide for a useful tool in many areas of research involving pulsed coils.

Good luck and enjoy,

Sincerely,
Darren (z_p_e)

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zeropoint electronics

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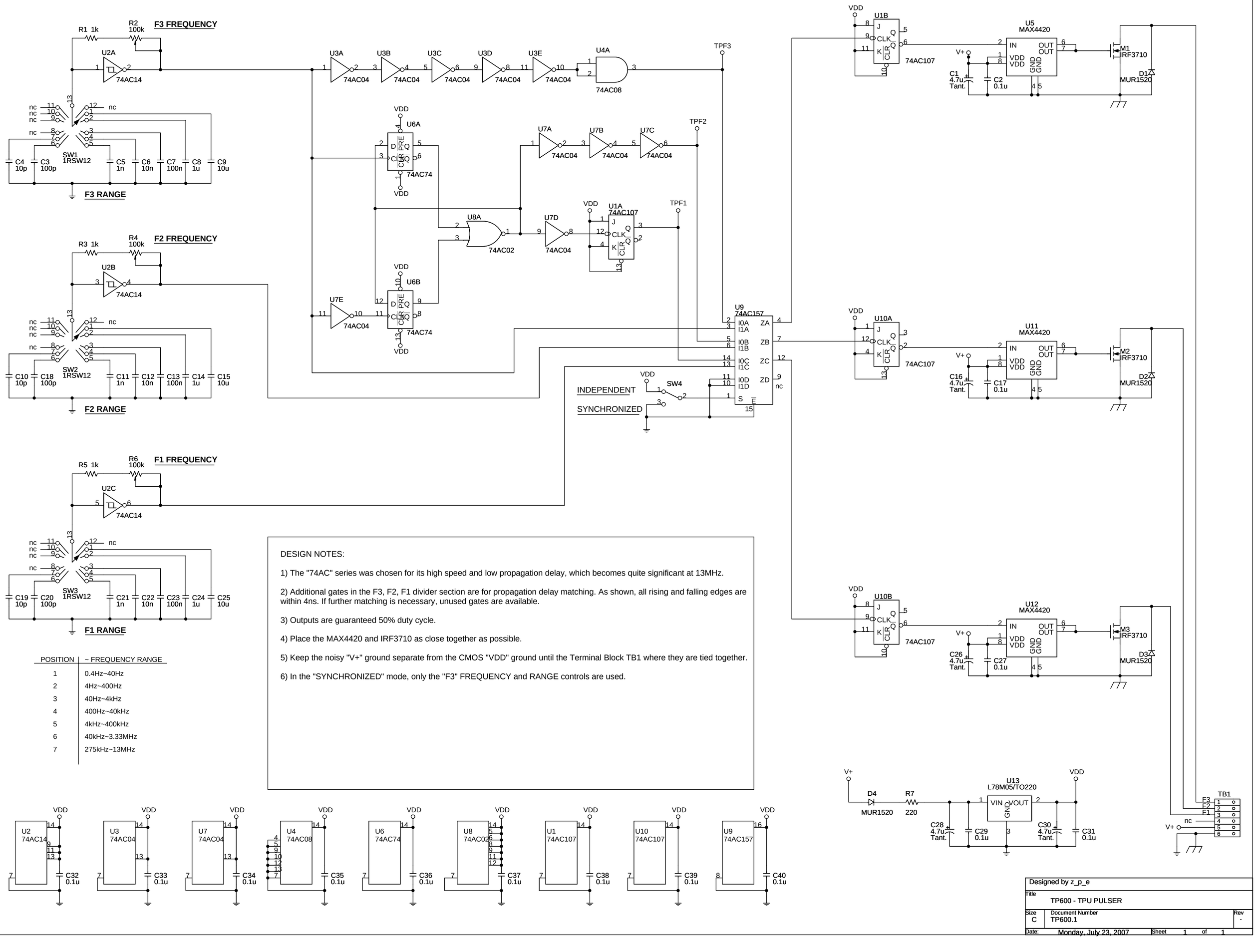
Item	Quantity	Reference	Part
1	5	C1,C16,C26,C28,C30	4.7u Tantalum
2	5	C2,C17,C27,C29,C31	0.1u Film, Mono, or Ceramic
3	3	C3,C18,C20	100p
4	3	C4,C10,C19	10p
5	3	C5,C11,C21	1n
6	3	C6,C12,C22	10n
7	3	C7,C13,C23	100n
8	3	C8,C14,C24	1u Film
9	3	C9,C15,C25	10u Film
10	4	D1,D2,D3,D4	MUR1520 Diode, Ultrafast
11	3	M1,M2,M3	IRF3710 Power MOSFET
12	3	R1,R3,R5	1k
13	3	R2,R4,R6	100k Potentiometer
14	1	R7	220
15	3	SW1,SW2,SW3	Rotary Switch, 12-position
16	1	SW4	Switch, SPDT
17	1	TB1	Terminal Block, 6-position
18	2	U1,U10	74AC107 Dual "JK" Flip-Flop
19	1	U2	74AC14 Hex Schmitt Inverter
20	2	U3,U7	74AC04 Hex Inverter
21	1	U4	74AC08 Quad "AND" Gate
22	3	U5,U11,U12	MAX4420 MOSFET Driver, Low-side
23	1	U6	74AC74 Dual "D" Flip-Flop
24	1	U8	74AC02 Quad "NOR" Gate
25	1	U9	74AC157 Quad Data Multiplexer
26	1	U13	L78M05/TO220 5V Regulator
27	9	C32-C40	0.1u Mono or Ceramic
28	3	HS1-HS3	Heat Sink, suitable for MOSFETs



POSITION	~ FREQUENCY RANGE
1	0.4Hz~40Hz
2	4Hz~400Hz
3	40Hz~4kHz
4	400Hz~40kHz
5	4kHz~400kHz
6	40kHz~3.33MHz
7	275kHz~13MHz

DESIGN NOTES:

1) The "74AC" series was chosen for its high speed and low propagation delay, which becomes quite significant at 13MHz.

2) Additional gates in the F3, F2, F1 divider section are for propagation delay matching. As shown, all rising and falling edges are within 4ns. If further matching is necessary, unused gates are available.

3) Outputs are guaranteed 50% duty cycle.

4) Place the MAX4420 and IRF3710 as close together as possible.

5) Keep the noisy "V+" ground separate from the CMOS "VDD" ground until the Terminal Block TB1 where they are tied together.

6) In the "SYNCHRONIZED" mode, only the "F3" FREQUENCY and RANGE controls are used.

Designed by	z_p_e
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